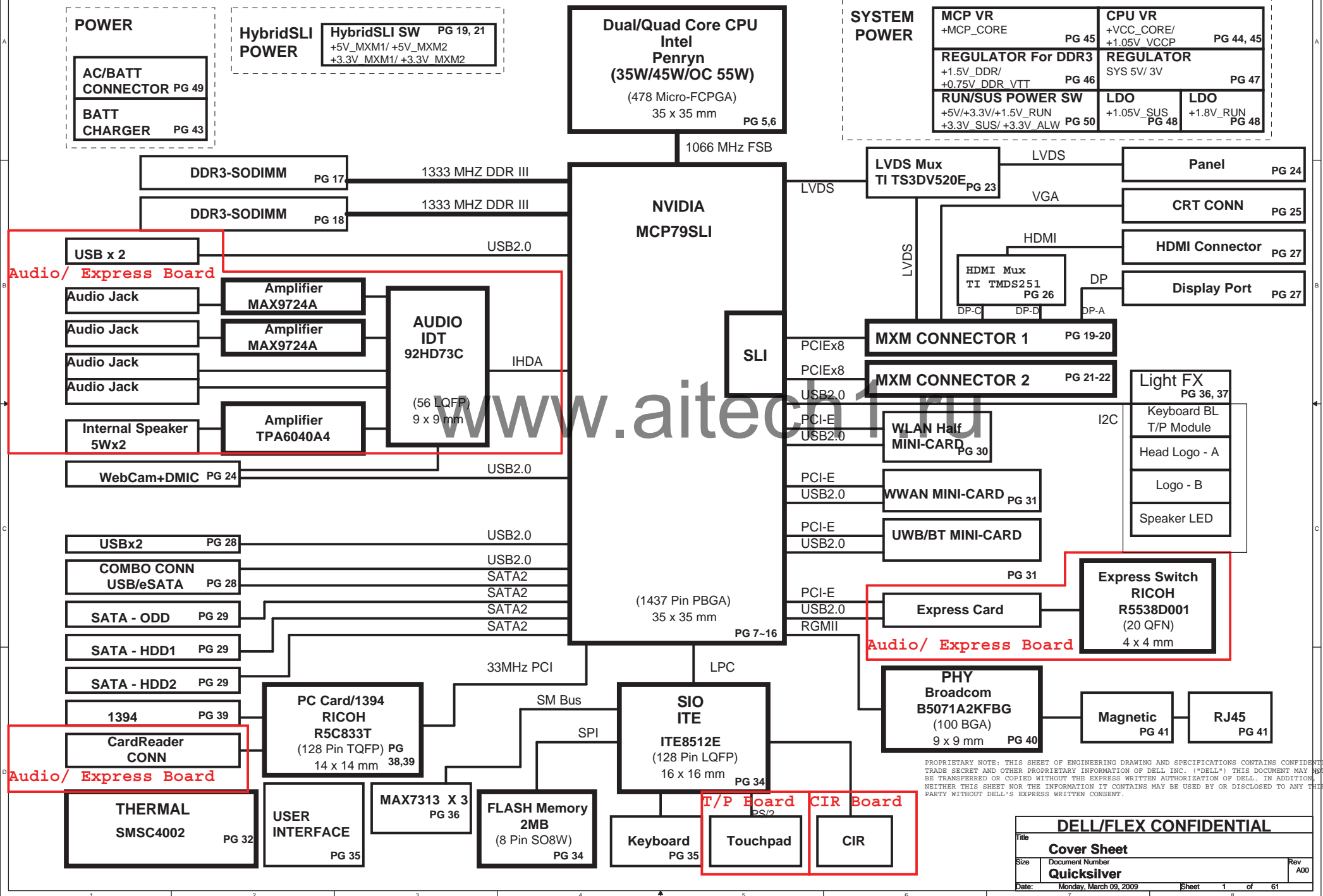


Quicksilver Design



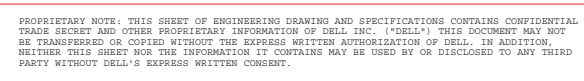
INDEX	
Page#	Description
1	Schematic Block Diagram
2	Front Page
3	PCI RESET/CLOCK
4	POWER SEQUENCING
5-6	Penryn
7-16	MCP79
17-18	DDRIII SO-DIMM(204P)
19-22	MXM CONN
23	LCD Conn. & SSP
25	CRT Conn
26	DeMux (SN75DP122)
27	HDMI & DP CONN
28	USBx2 & eSATA
29	SATA & IDE Conn
30	Mini Card (WLAN)
31	MINI-CARD (WPAN,WWAN)
32	FAN & Thermal
33	SIO (ITE8512)
34	Flash ROM, RTC & CIR
35	Keyboard, Daughtor Board conn & User Interface
36, 37	LED Light FX
38, 39	PCCARD/Conn & 1394
40,41	PHY(B5071), RJ45 & Transform
42	System Reset Circuit
43	CHARGER (MAX8731)
44	CPU Core (MAX8786)
45	MCP79, 1.05VCC (MAX17007)
46	DDR3 1.5V/0.75V(TPS51116)
47	SYS 5V/3V(MAX17020)
48	1.05V_SUS/ 1.8V_RUN
49	DCIN,Batt
50	RUN POWER SW
51	Power Diagram
52	PAD& SCREW
53	PCI Reset Map

Power States									
Power Rail	Control Signal	S0	S3	S4	S5	G3	S4/ M-off	S5/ M-off	
+PWR_SRC	N/A	V	V	V	V	V			
+0.75V_DDR_VTT	RUN_ON	V							
+1.05V_VCCP	CPUVDD_EN	V							
+1.05V_RMGT	SLP_RMGT#	V							
+1.05V_SUS	SUS_ON	V	V						
+1.5V_RUN	RUN_ON	V							
+1.5V_DDR	SUS_ON	V	V						
+1.8V_RUN	RUN_ON	V							
+15V_ALW	N/A	V	V	V	V	V			
+3.3V_ALW	+3.3V_EN2	V	V	V	V	V			
+3.3V_RMGT	SLP_RMGT#	V							
+3.3V_RUN	RUN_ON	V							
+3.3V_SUS	SUS_ON	V	V						
+5V_ALW	+5V_EN1	V	V	V	V	V			
+5V_ALW2	N/A	V	V	V	V	V			
+5V_SUS	SUS_ON	V	V						
+5V_HDD	HDDC_EN	V	TBD						
+5V_MOD	MODC_EN	V	TBD						
+5V_RUN	RUN_ON	V							
+GFX_PWR_SRC	N/A	V	V	V	V	V			
+LCDVCC	ENVDD	V							
+MCP_CORE	RUN_ON	V							
+RTC_CELL	RTC	V	V	V	V	V			
+VCC_CORE	1.05V_VCCP_PWRGD	V							
+USB_RIGHT_PWR	USB_SIDE_EN#	V	TBD						
+USB_LEFT_PWR	USB_BACK_EN#	V	TBD						

By Anthony

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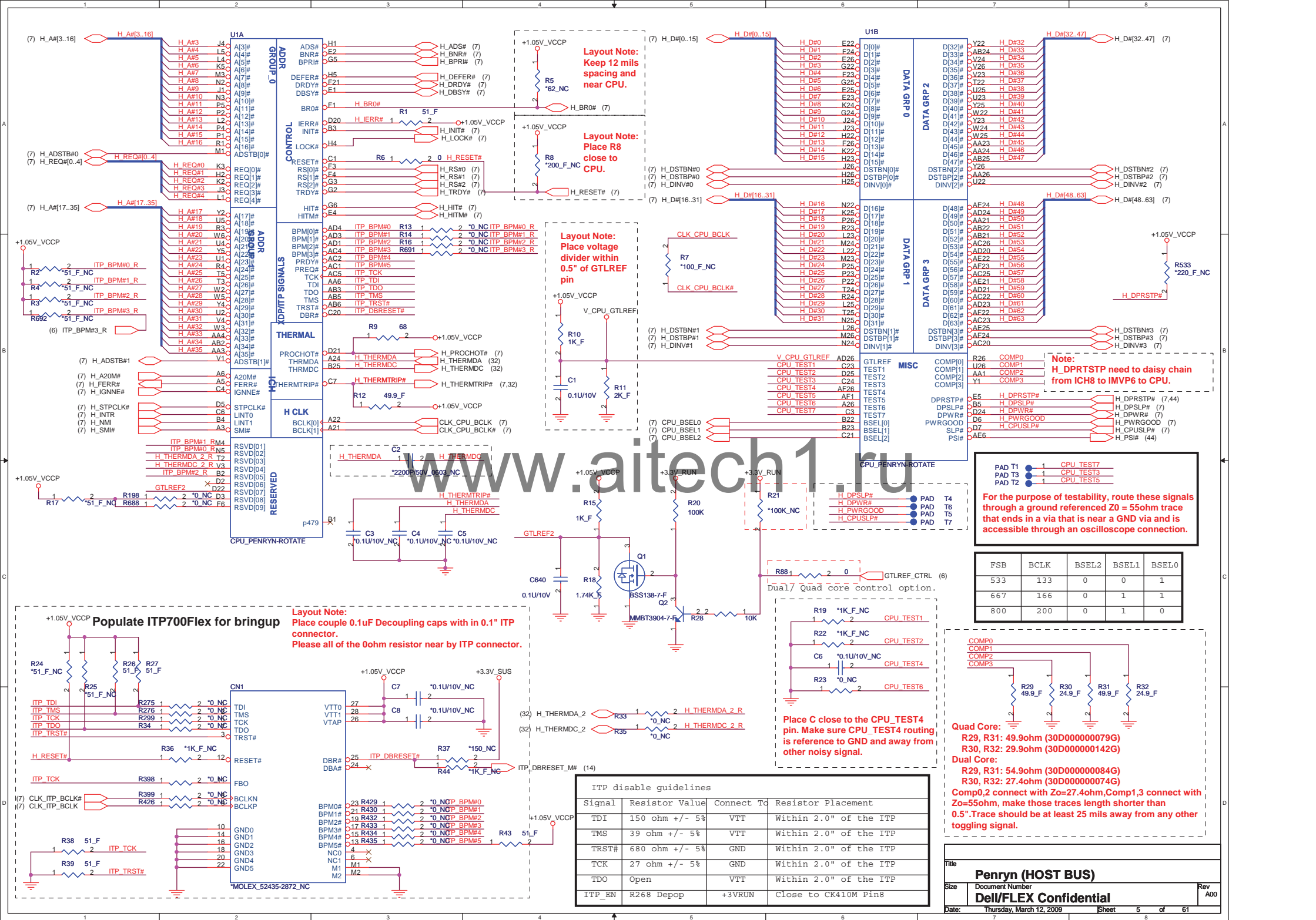
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Size	Document Number	Dell/FLEX Confidential	
Date:	Monday, March 09, 2009	Sheet	2 of 61
Rev		A00	

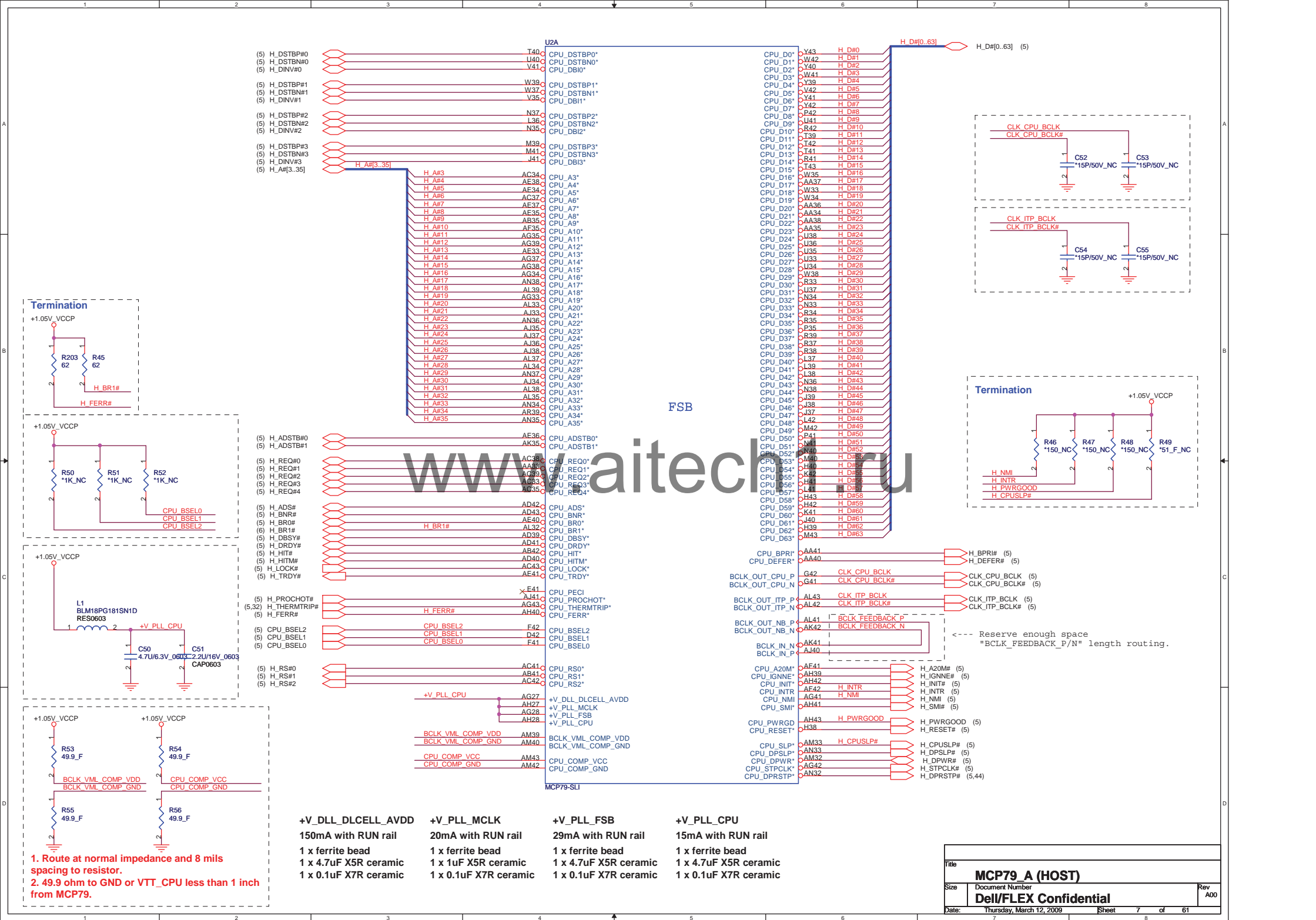


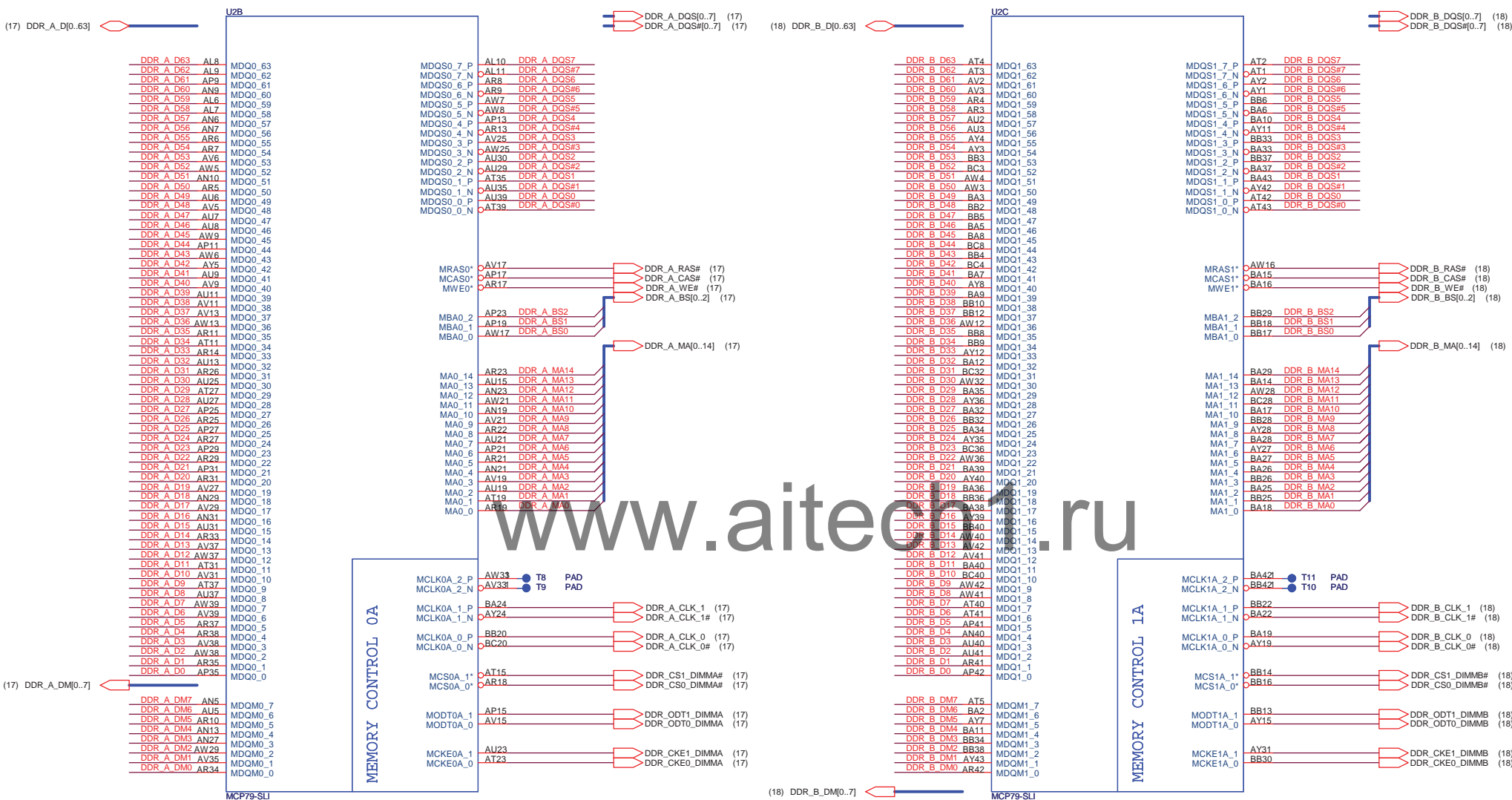
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(19) PCIE_MRX_GTX_P[0..7]
(19) PCIE_MRX_GTX_N[0..7]
(21) PCIE_MRX_GTX_P[8..15]
(21) PCIE_MRX_GTX_N[8..15]

PCIE Layout Notice:
MCP79 BGA Breakout (<27ps):
Route at 50 ohm impedance and 1.5x dielectric height spacing.
After Breakout:
Route at 50 Signal end and 90 ohm differential.
Inter-pair spacing 4x (Microstrip) dielectric height spacing 3x (Stripline) dielectric height spacing.

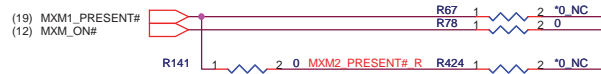
PCIE MRX GTX P0 E7
PCIE MRX GTX N0 E7
PCIE MRX GTX P1 D7
PCIE MRX GTX N1 C7
PCIE MRX GTX P2 E6
PCIE MRX GTX N2 E6
PCIE MRX GTX P3 E5
PCIE MRX GTX N3 F5
PCIE MRX GTX P4 E4
PCIE MRX GTX N4 E3
PCIE MRX GTX P5 D3
PCIE MRX GTX N5 C3
PCIE MRX GTX P6 G5
PCIE MRX GTX N6 H5
PCIE MRX GTX P7 J7
PCIE MRX GTX N7 J6
PCIE MRX GTX P8 J5
PCIE MRX GTX N8 J4
PCIE MRX GTX P9 L11
PCIE MRX GTX N9 L10
PCIE MRX GTX P10 L9
PCIE MRX GTX N10 L8
PCIE MRX GTX P11 L7
PCIE MRX GTX N11 L6
PCIE MRX GTX P12 N11
PCIE MRX GTX N12 N10
PCIE MRX GTX P13 N9
PCIE MRX GTX N13 N8
PCIE MRX GTX P14 N7
PCIE MRX GTX N14 N6
PCIE MRX GTX P15 N5
PCIE MRX GTX N15 N4

PCIE

PE0_TX0_P C5
PE0_TX0_N D4
PE0_TX1_P C4
PE0_TX1_N B4
PE0_TX2_P A4
PE0_TX2_N B3
PE0_TX3_P B2
PE0_TX3_N C1
PE0_TX4_P D1
PE0_TX4_N D2
PE0_TX5_P E1
PE0_TX5_N E2
PE0_TX6_P F2
PE0_TX6_N F3
PE0_TX7_P G4
PE0_TX7_N G3
PE0_TX8_P H4
PE0_TX8_N H3
PE0_TX9_P H2
PE0_TX9_N H1
PE0_TX10_P J1
PE0_TX10_N J2
PE0_TX11_P J3
PE0_TX11_N K2
PE0_TX12_P K3
PE0_TX12_N L4
PE0_TX13_P L3
PE0_TX13_N M4
PE0_TX14_P M3
PE0_TX14_N M2
PE0_TX15_P M1
PE0_TX15_N M1

PCIE MTX GRX C P0 C81
PCIE MTX GRX C N0 C74
PCIE MTX GRX C P1 C82
PCIE MTX GRX C N1 C83
PCIE MTX GRX C P2 C85
PCIE MTX GRX C N2 C84
PCIE MTX GRX C P3 C75
PCIE MTX GRX C N3 C86
PCIE MTX GRX C P4 C76
PCIE MTX GRX C N4 C88
PCIE MTX GRX C P5 C87
PCIE MTX GRX C N5 C89
PCIE MTX GRX C P6 C91
PCIE MTX GRX C N6 C90
PCIE MTX GRX C P7 C93
PCIE MTX GRX C N7 C92
PCIE MTX GRX C P8 C77
PCIE MTX GRX C N8 C94
PCIE MTX GRX C P9 C96
PCIE MTX GRX C N9 C95
PCIE MTX GRX C P10 C97
PCIE MTX GRX C N10 C99
PCIE MTX GRX C P11 C98
PCIE MTX GRX C N11 C101
PCIE MTX GRX C P12 C100
PCIE MTX GRX C N12 C78
PCIE MTX GRX C P13 C102
PCIE MTX GRX C N13 C79
PCIE MTX GRX C P14 C103
PCIE MTX GRX C N14 C104
PCIE MTX GRX C P15 C80
PCIE MTX GRX C N15 C105

PCIE_MTX_GRX_P[0..7] (19)
PCIE_MTX_GRX_N[0..7] (19)
PCIE_MTX_GRX_P[8..15] (21)
PCIE_MTX_GRX_N[8..15] (21)



Express Card (39) CARD_CLK_REQ#
(33,39) EXPRCRD_PWREN#

WLAN (30) MINI1CLK_REQ#

PPU (31) MINI2CLK_REQ#

WWAN (31) MINI3CLK_REQ#

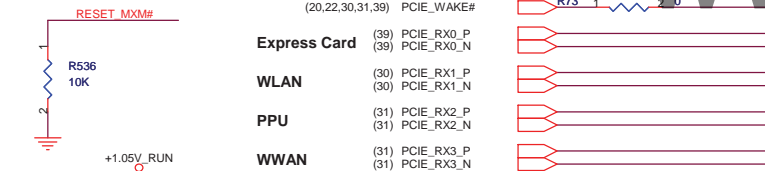
(19,21,26) PE_RESET_MXM#
(21,33) MXM2_PRESENT#
+3.3V_RUN
(22) MXM2_PWROK
(20,33) MXM1_PWROK
+3.3V_RUN
(20,22,30,31,39) PCIE_WAKE#

Express Card (39) PCIE_RX0_P
(39) PCIE_RX0_N

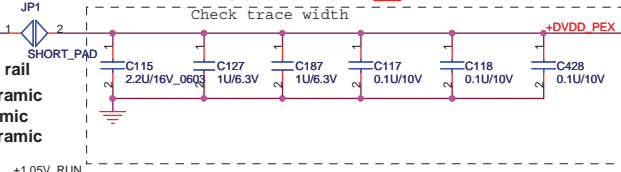
WLAN (30) PCIE_RX1_P
(30) PCIE_RX1_N

PPU (31) PCIE_RX2_P
(31) PCIE_RX2_N

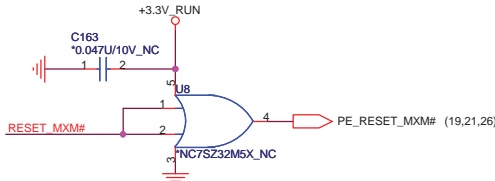
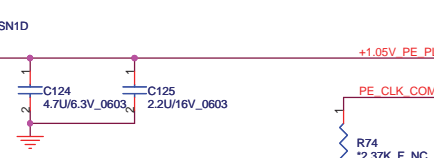
WWAN (31) PCIE_RX3_P
(31) PCIE_RX3_N



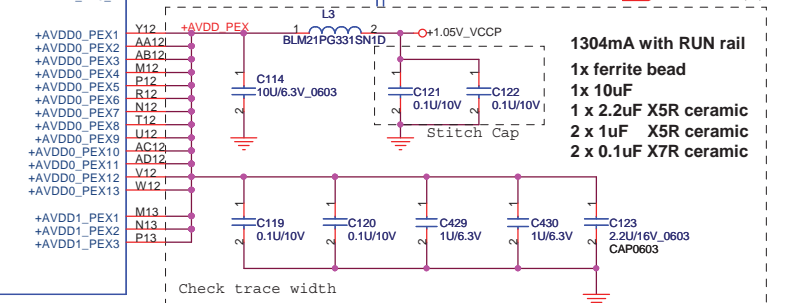
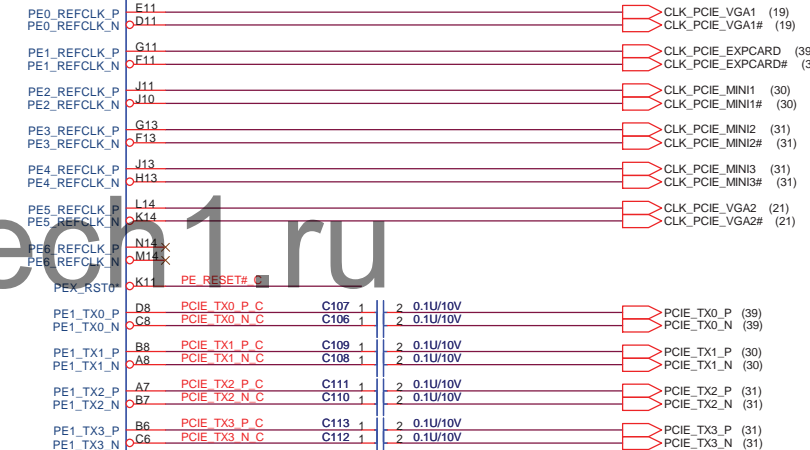
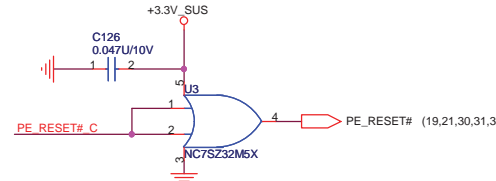
482mA with RUN rail
1 x 2.2uF X5R ceramic
2 x 1uF X5R ceramic
2 x 0.1uF X7R ceramic



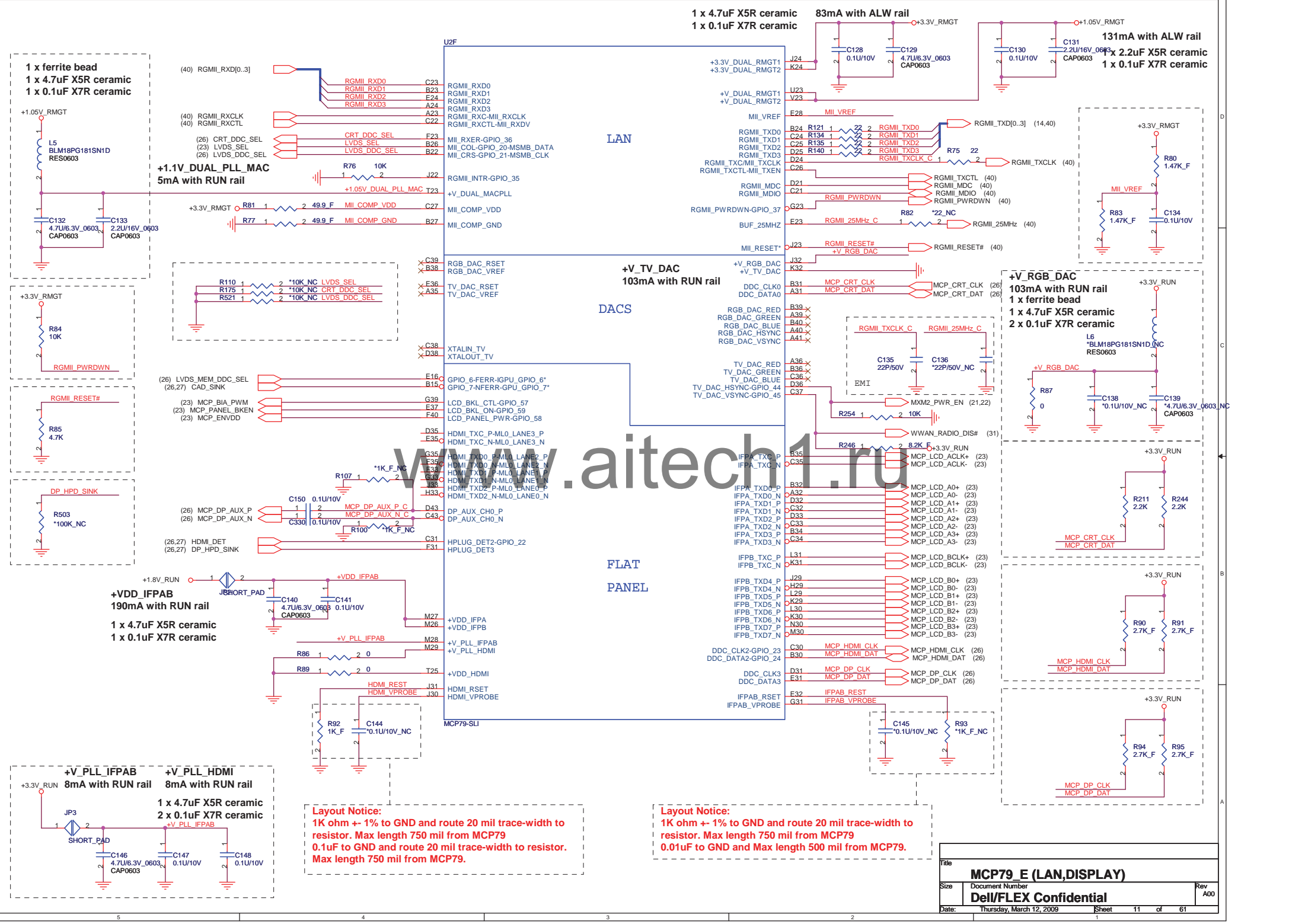
202mA with RUN rail
1 x ferrite bead
1 x 4.7uF X5R ceramic
1 x 0.1uF X7R ceramic



Layout Notice:
1. 2.37K ohm to GND within 500 mil of MCP79
2. Route an nominal impedance or wider trace and 8 mil spacing to resistor.



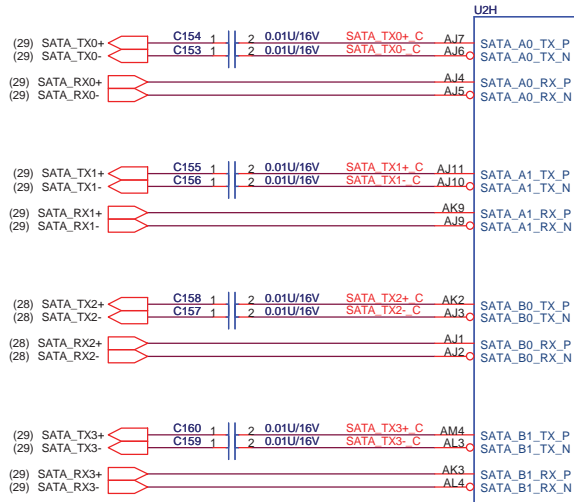
1304mA with RUN rail
1x ferrite bead
1x 10uF
1 x 2.2uF X5R ceramic
2 x 1uF X5R ceramic
2 x 0.1uF X7R ceramic



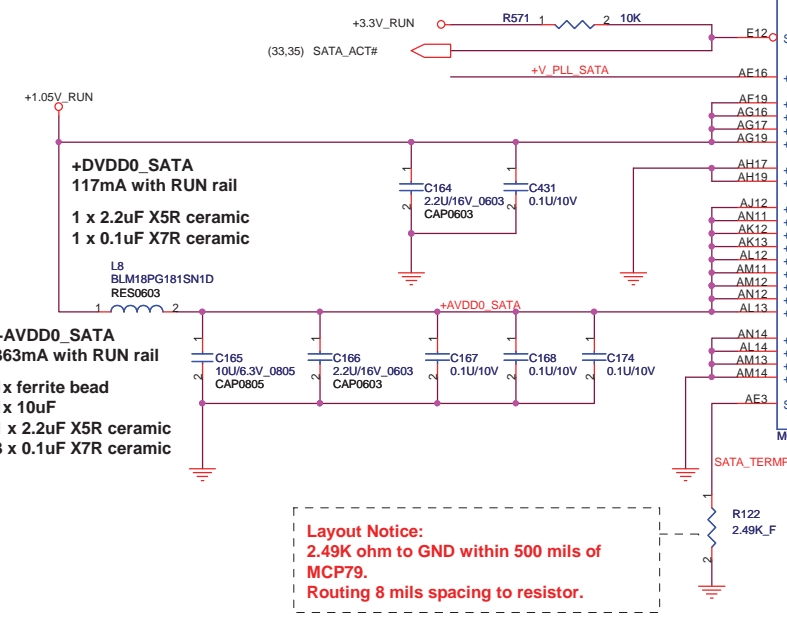
Layout Notice:
1K ohm +/- 1% to GND and route 20 mil trace-width to resistor. Max length 750 mil from MCP79
0.1uF to GND and route 20 mil trace-width to resistor. Max length 750 mil from MCP79.

Layout Notice:
1K ohm +/- 1% to GND and route 20 mil trace-width to resistor. Max length 750 mil from MCP79
0.01uF to GND and Max length 500 mil from MCP79.

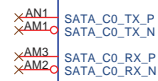
Title		
MCP79 E (LAN,DISPLAY)		
Size	Document Number	Rev
	Del/FLEX Confidential	A00
Date:	Thursday, March 12, 2009	Sheet 11 of 61



SATA Layout Notice:
BGA Breakout:
Route differentially at normal impedance and 4 mils within pair and 6 mils to other signals. Maximum breakout distance is 400 mils of MCP79.
BGA Fan-out:
Route differentially at normal impedance and 4 mils within pair and 10 mils to other signals. Maximum BGA breakout plus Fan-out distance is 500 mils.
After Breakout:
Route at 100 ohm differential impedance (50 ohm SE) and 3x dielectric height spacing to other signals.
TX and RX intra-pair skew for a differential pair is 5 mils.



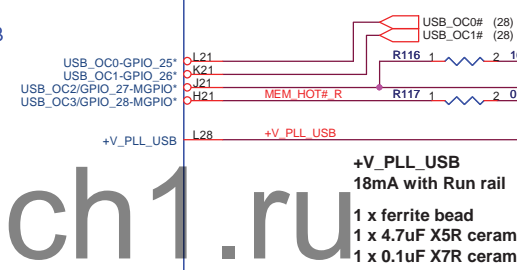
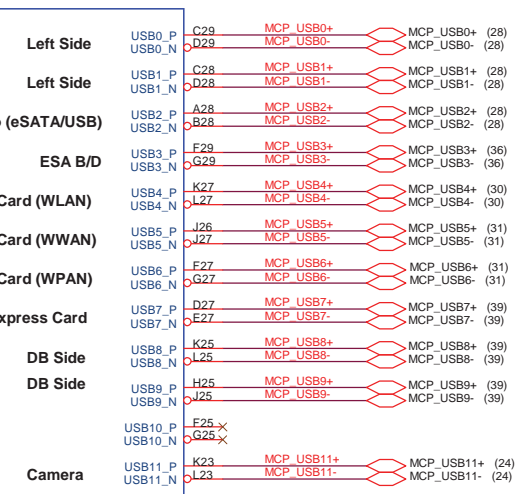
Layout Notice:
2.49K ohm to GND within 500 mils of MCP79.
Routing 8 mils spacing to resistor.



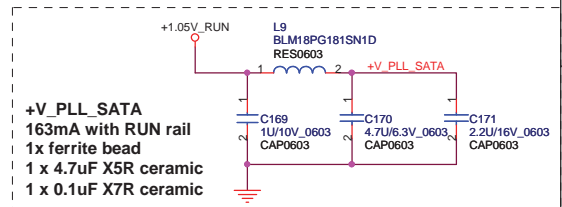
SATA

USB

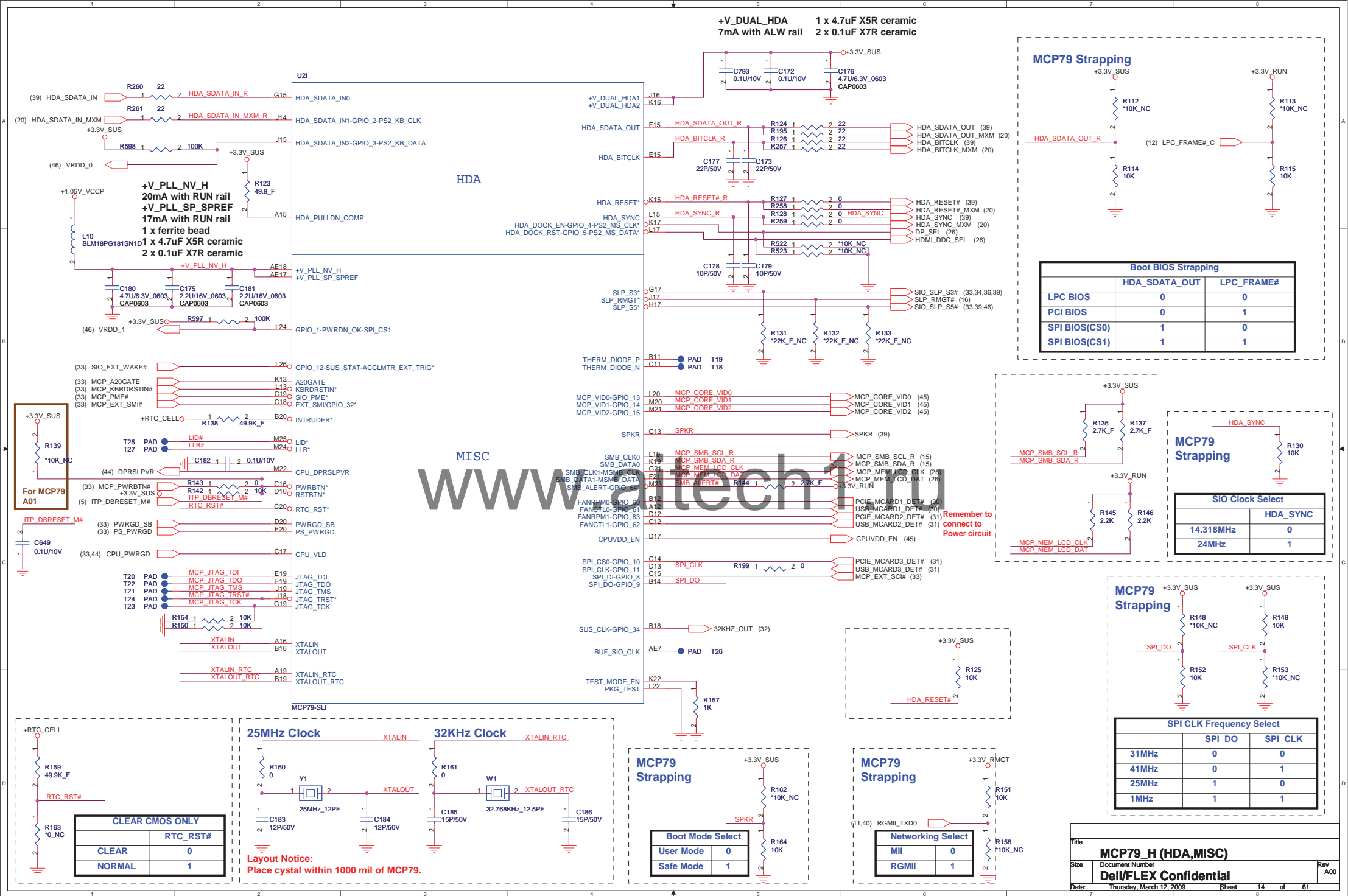
- Left Side
- Left Side
- Combo (eSATA/USB)
- ESA B/D
- Mini Card (WLAN)
- Mini Card (WWAN)
- Mini Card (WPAN)
- Express Card
- DB Side
- DB Side
- Camera



Layout Notice:
806 ohm +/-1% to GND within 1000 mil of MCP79.
Routing trace at least 8 mil wide to resistor.

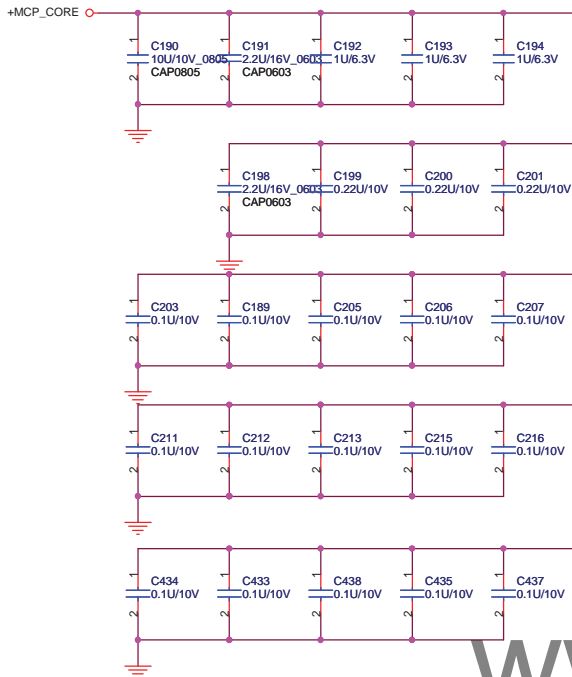


USB Layout Notice:
BGA Breakout:
Route differentially at normal impedance and 4 mils within pair and 6 mils to other signals. Maximum breakout distance is 300 mils of MCP79.
BGA Fan-out:
Route differentially at normal impedance and 4 mils within pair and 10 mils to other signals. Maximum BGA breakout plus Fan-out distance is 400 mils.
After Breakout:
Route at 100 ohm differential impedance (50 ohm SE) and 4x dielectric height spacing (Microstrip) or 2x dielectric height spacing (Stripline) to other signals.
Each USB pair must be length matched to within 50 mil.

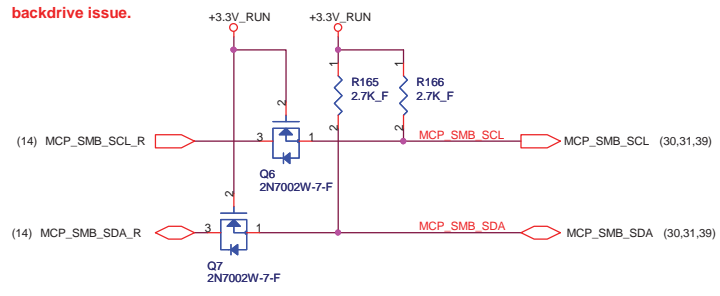


17.756A with RUN rail for S0
2850mA for S0 Idle

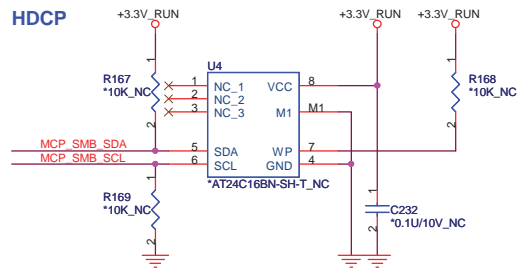
1 x 10uF ceramic
2 x 2.2uF X5R ceramic
3 x 1uF X5R ceramic
3 x 0.22uF X5R ceramic
12 x 0.1uF X7R ceramic



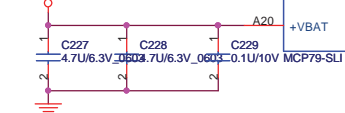
These are for
backdrive issue.



HDCP



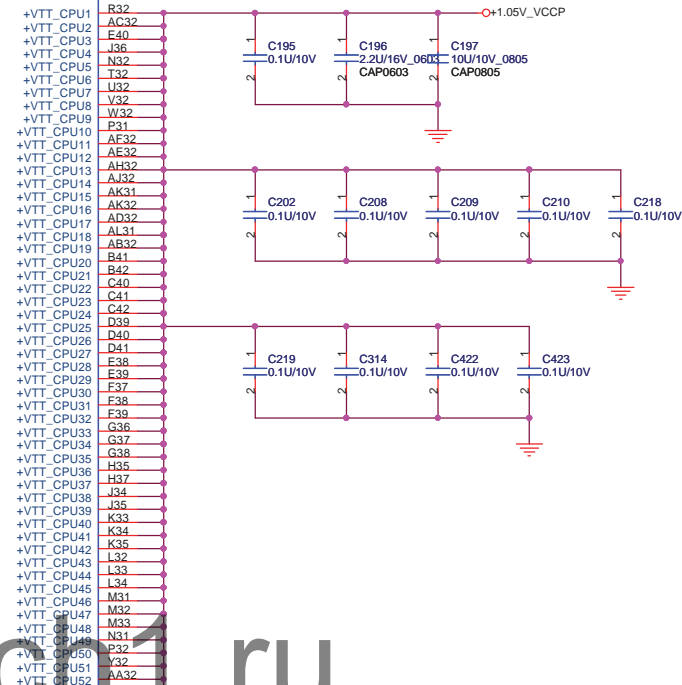
+RTC_CELL



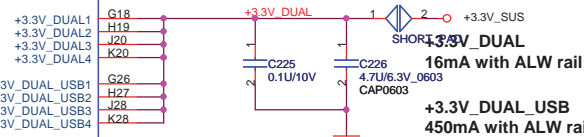
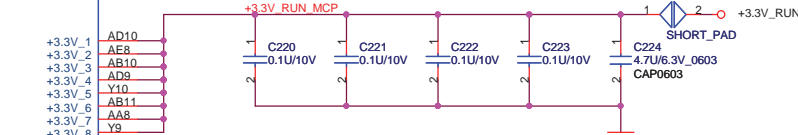
0.06mA with ALW rail for S0
2 x 4.7uF X5R ceramic
1 x 0.1uF X7R ceramic

PWR

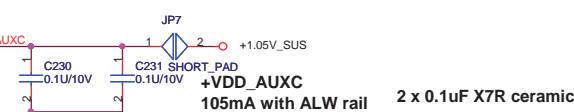
+VTT_CPU 1 x 10uF ceramic
1139mA for ALW rail 1 x 2.2uF X5R ceramic
+VTT_CPUCLK 43mA for ALW rail 3 x 0.1uF X7R ceramic



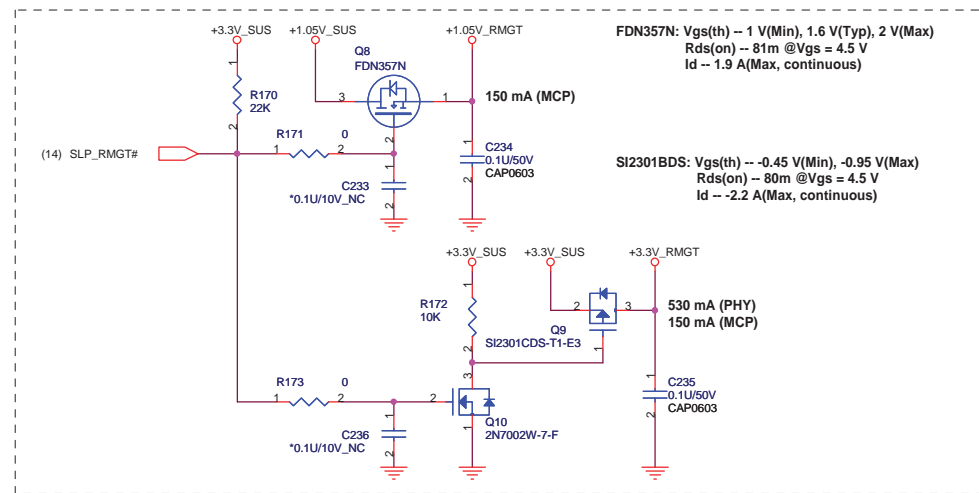
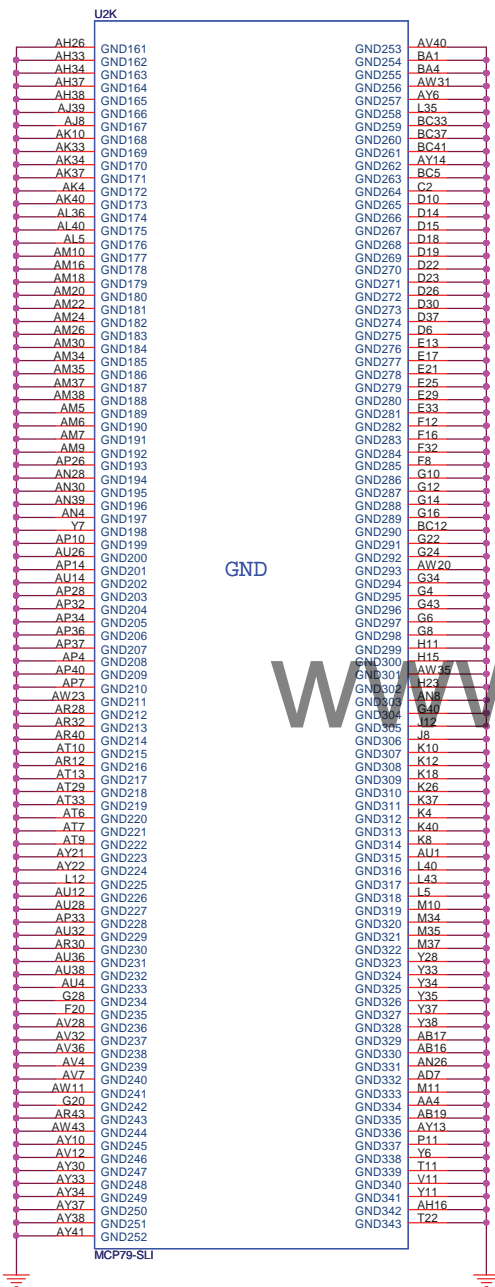
+3.3V_RUN_MCP 1 x 4.7uF X5R ceramic
450mA with RUN rail 4 x 0.1uF X7R ceramic



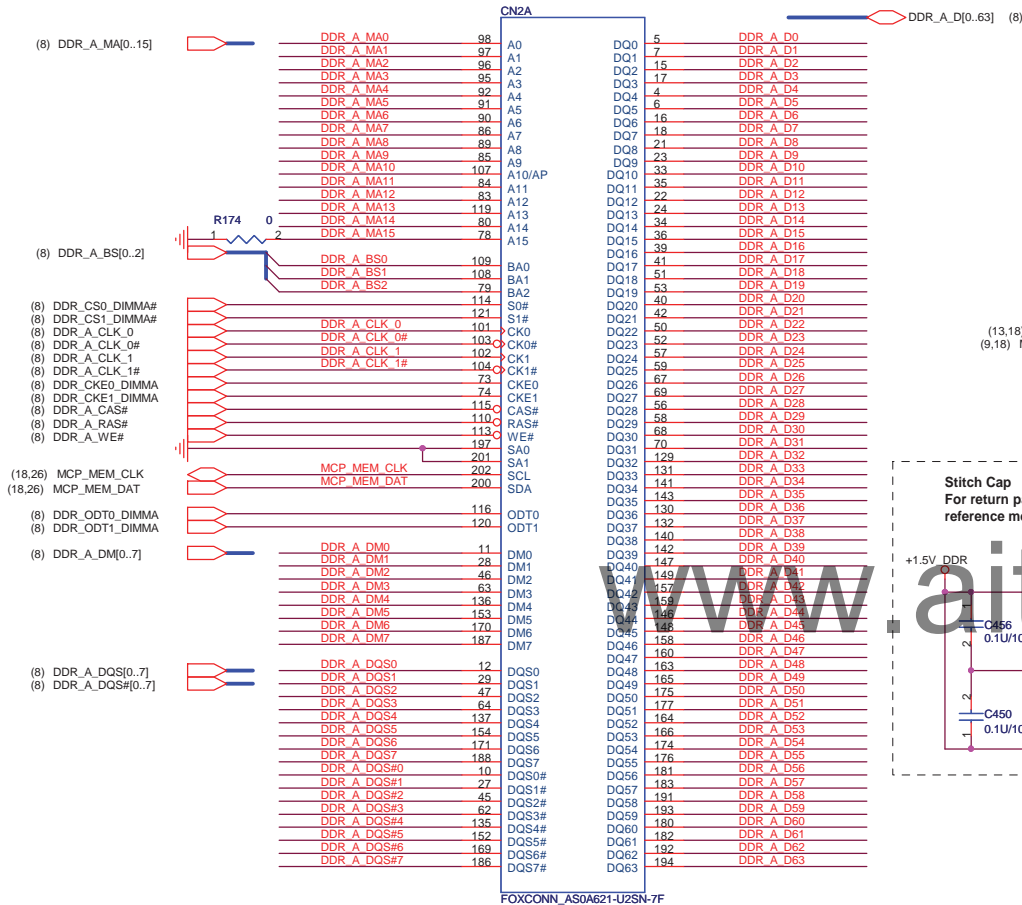
+3.3V_DUAL_USB 450mA with ALW rail



Title			
MCP79 I (POWER)			
Size			
Document Number			
Del/FLEX Confidential			
Date:			
Monday, March 09, 2009			
Sheet			
15 of 61			
Rev			
A00			



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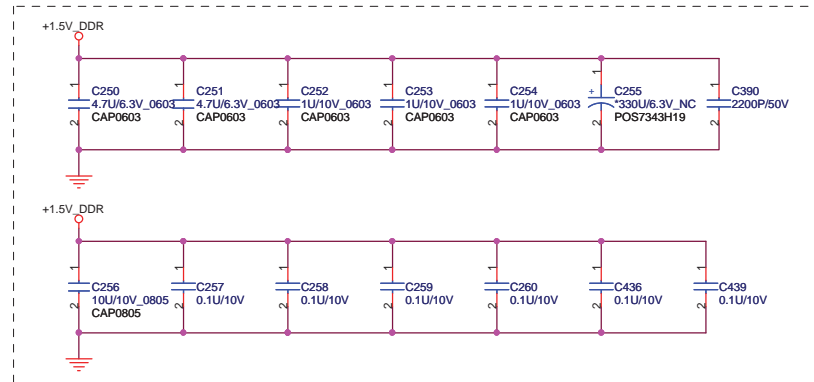
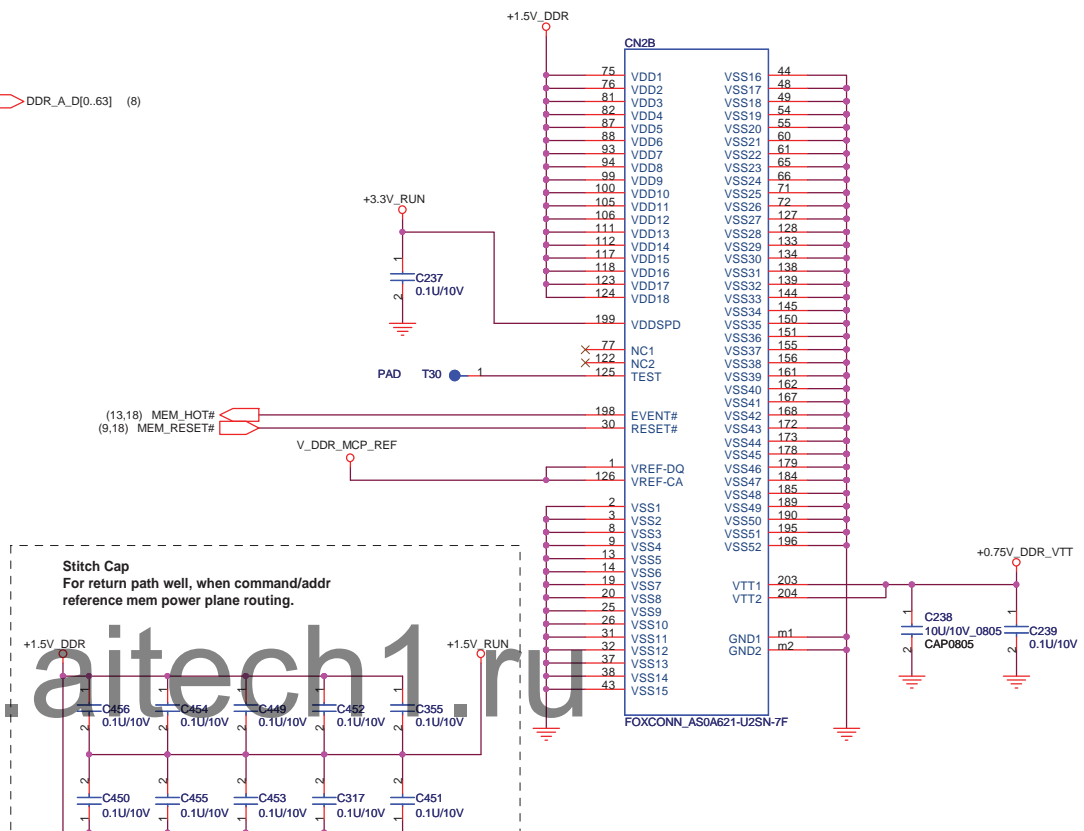
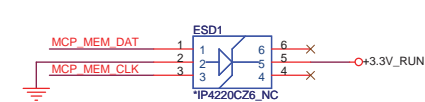
3/21 Neo: Update symbol.

SM_MEM BUS ADDRESS	
SO-DIMM0	1010 000
SO-DIMM1	1010 001

For EMI Reserved

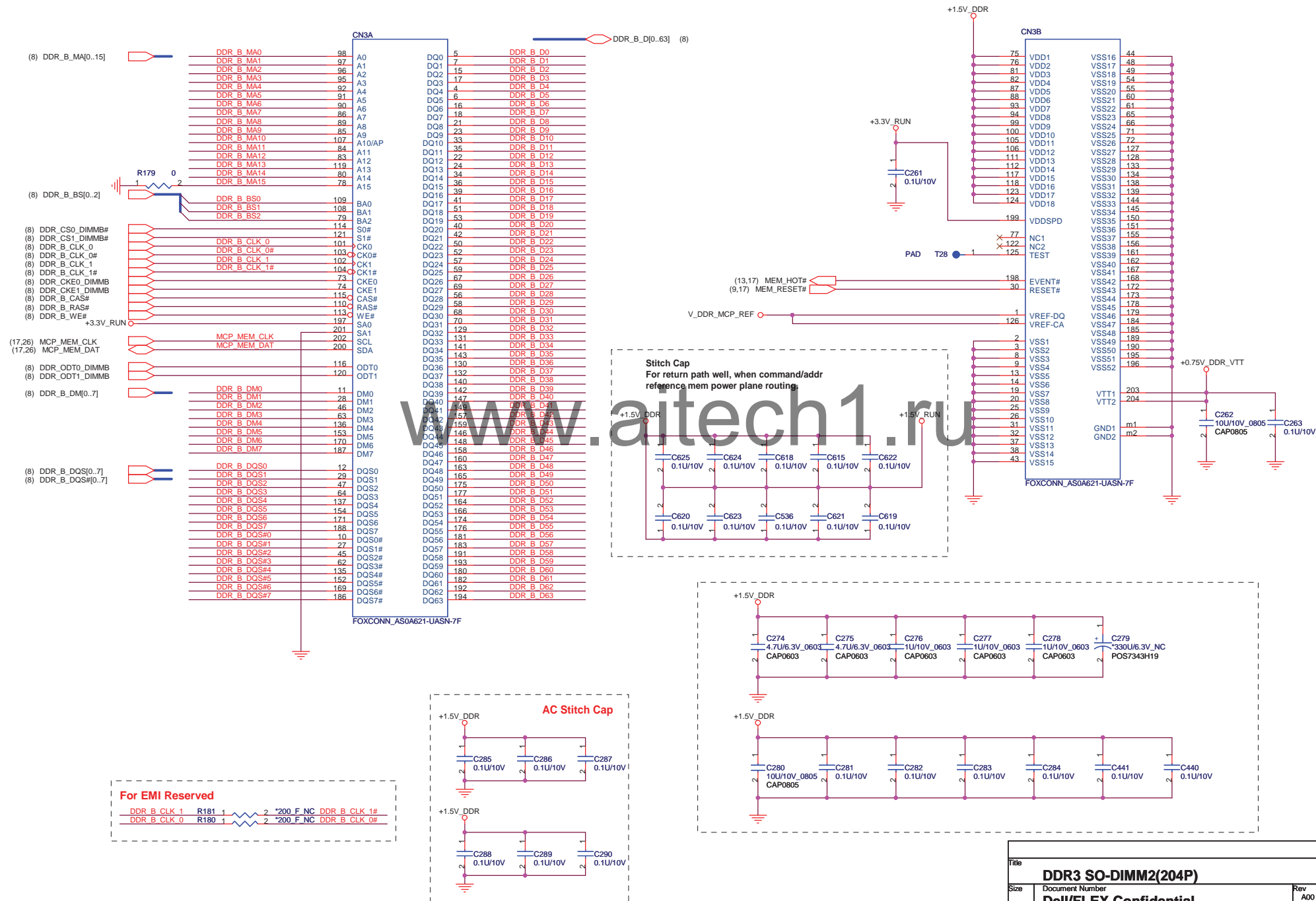
DDR_A_CLK_1 R178 1 2 *200 F_NC DDR_A_CLK_1#
DDR_A_CLK_0 R177 1 2 *200 F_NC DDR_A_CLK_0#

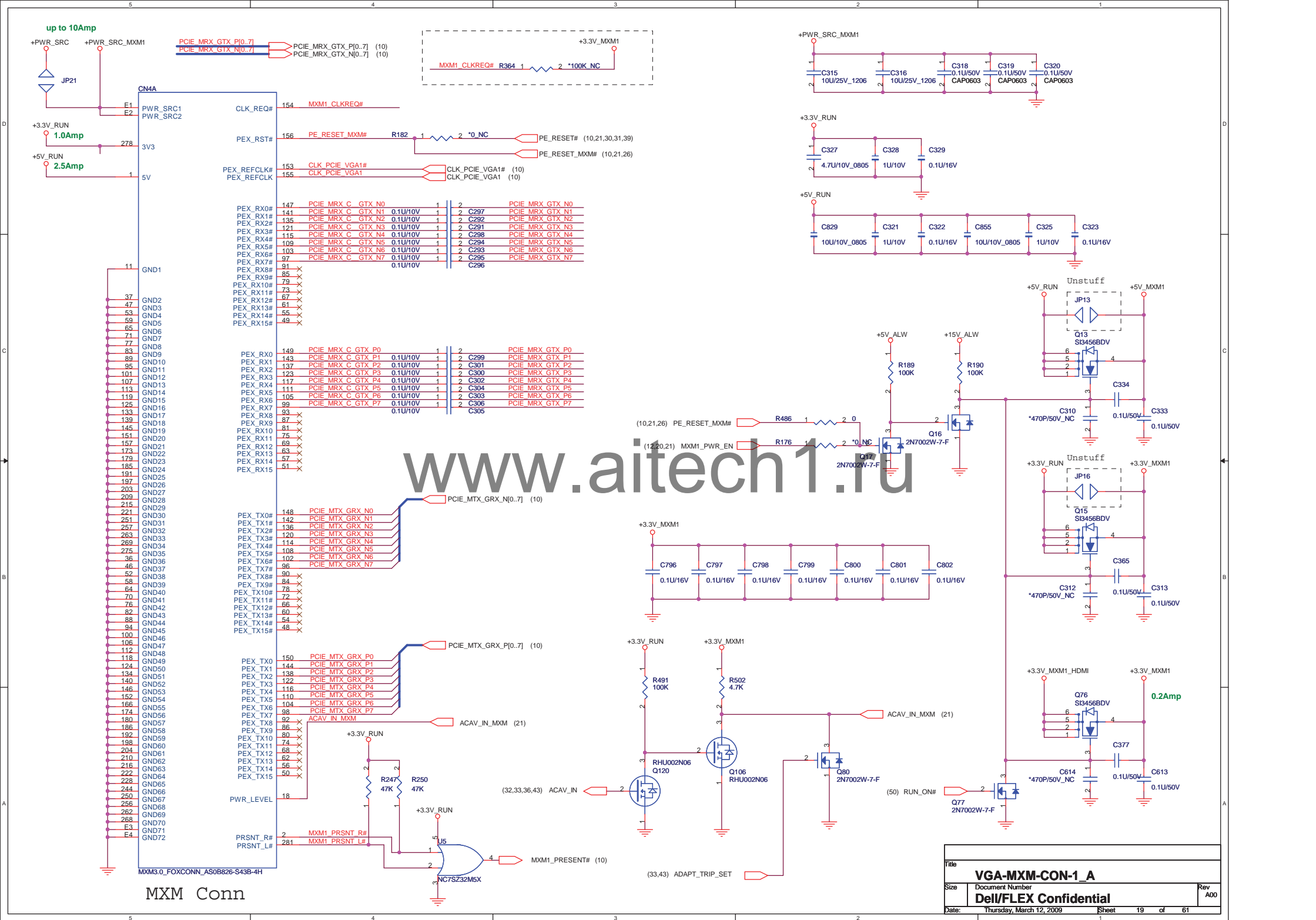
Place ESD Protection diodes.

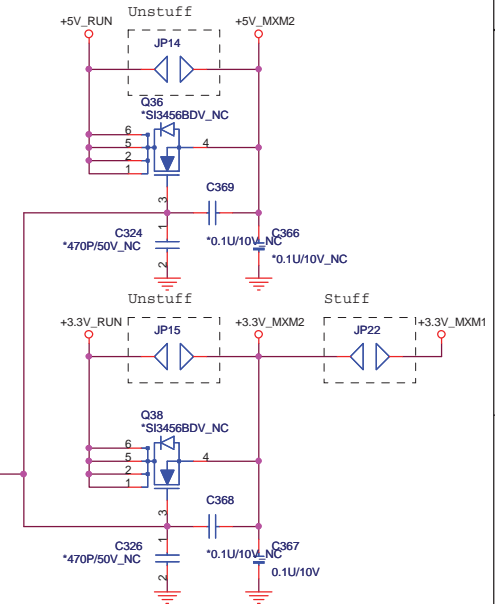
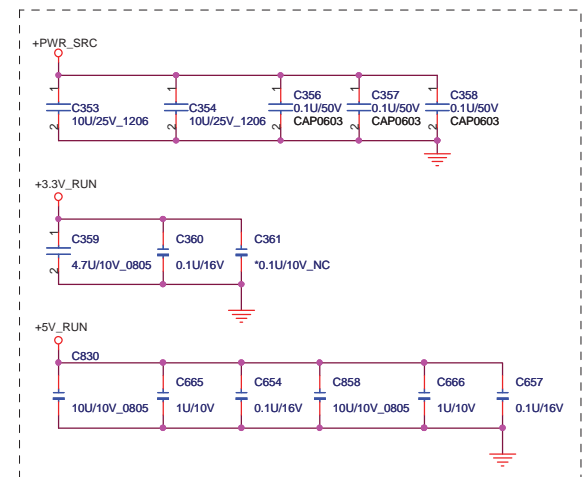
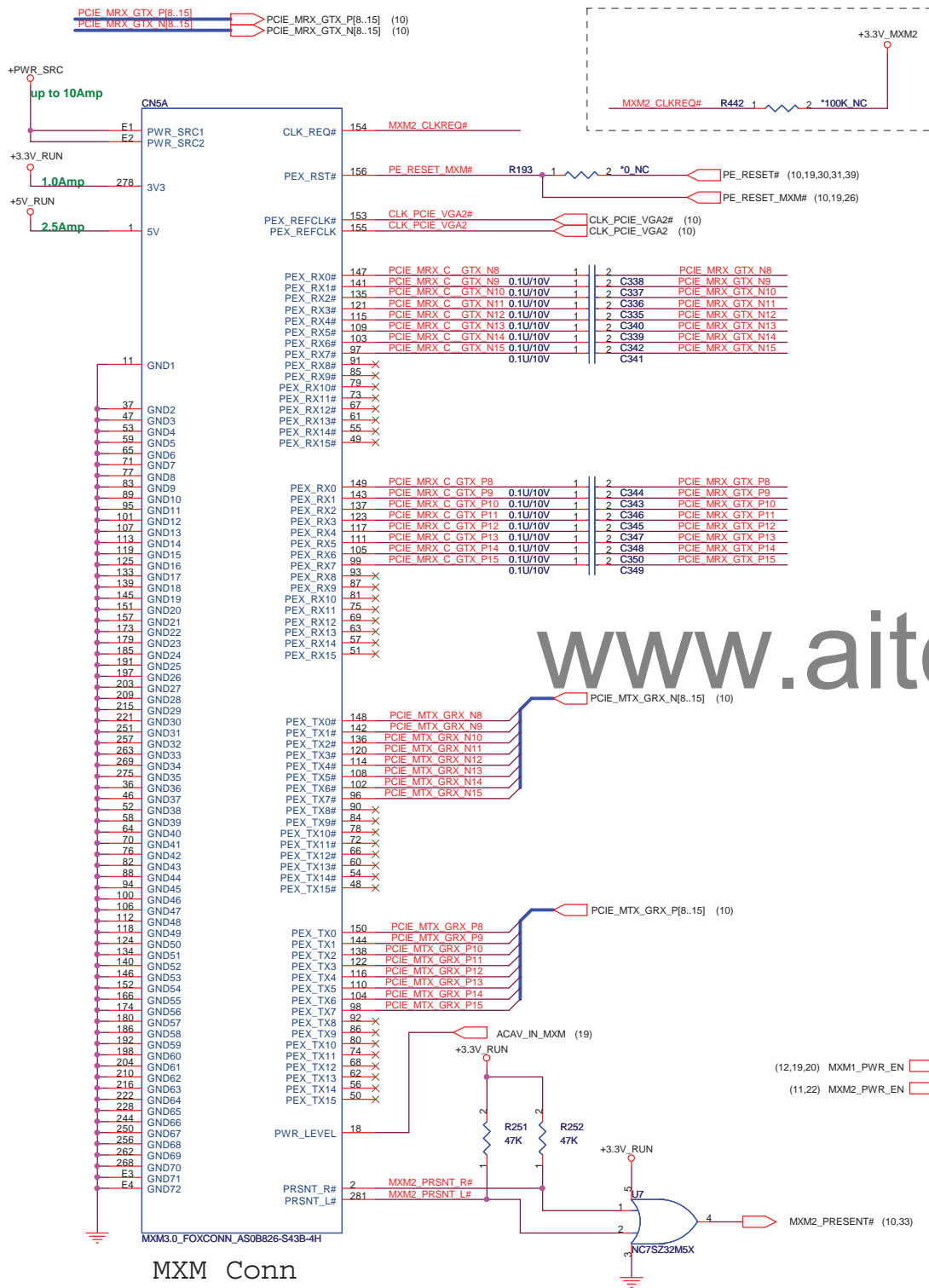


Title	DDR3 SO-DIMM1(204P)		
Size	Document Number	Rev A00	
Date:	Thursday, March 12, 2009	Sheet	17 of 61

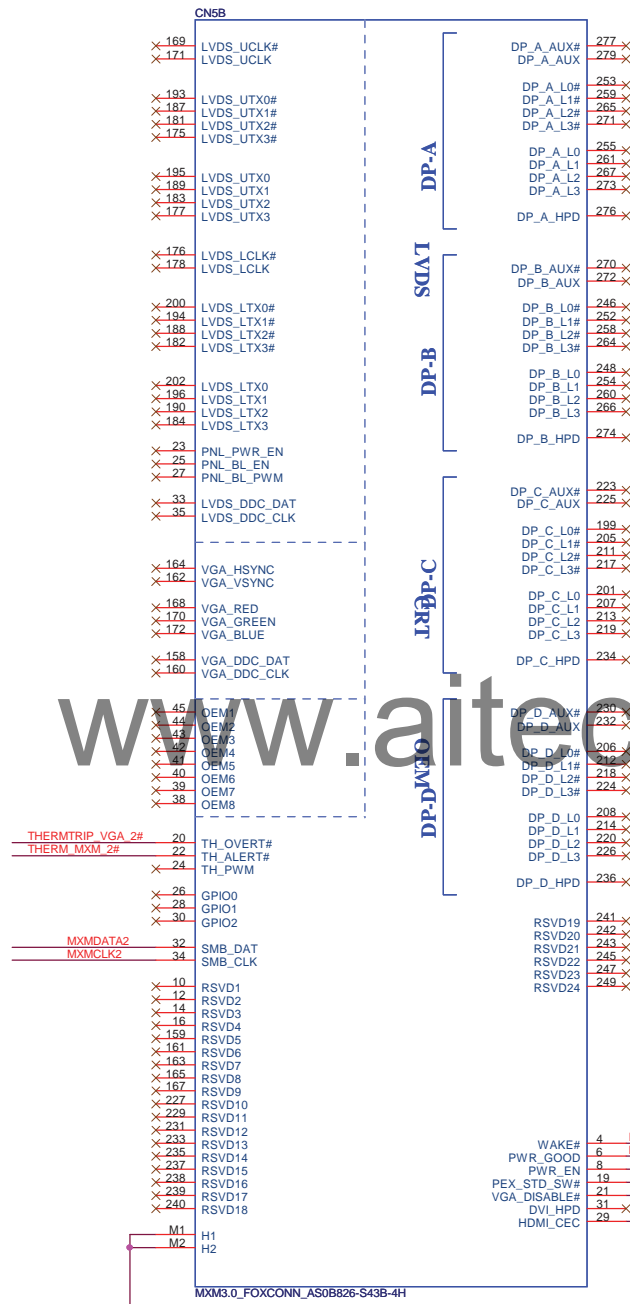
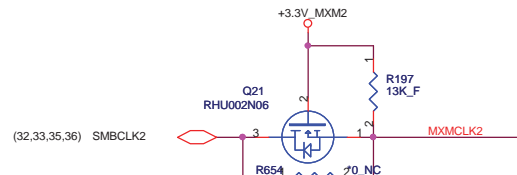
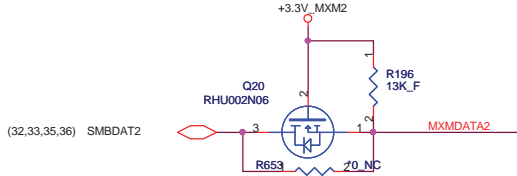
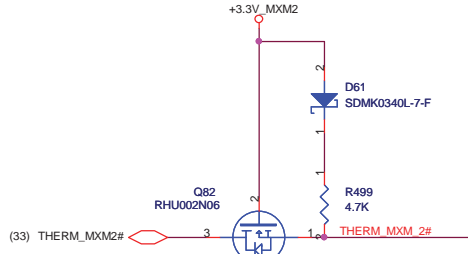
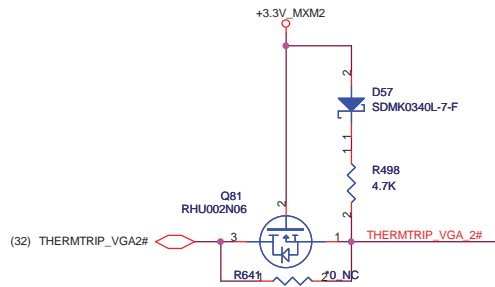
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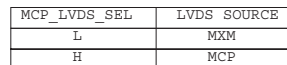
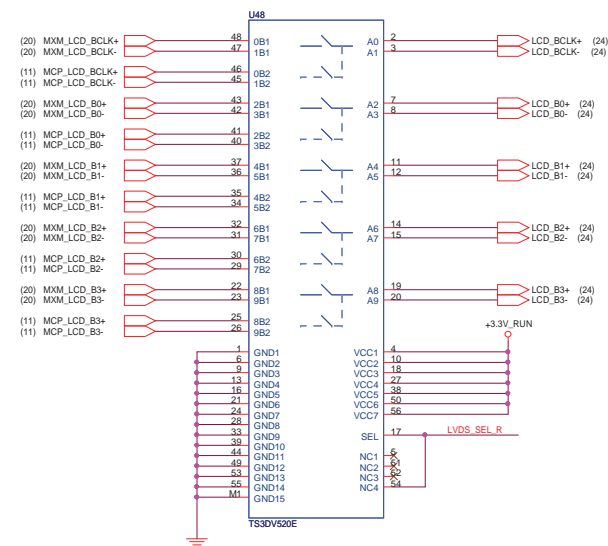




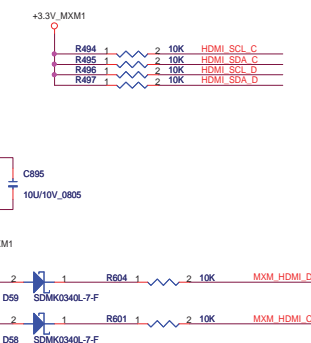


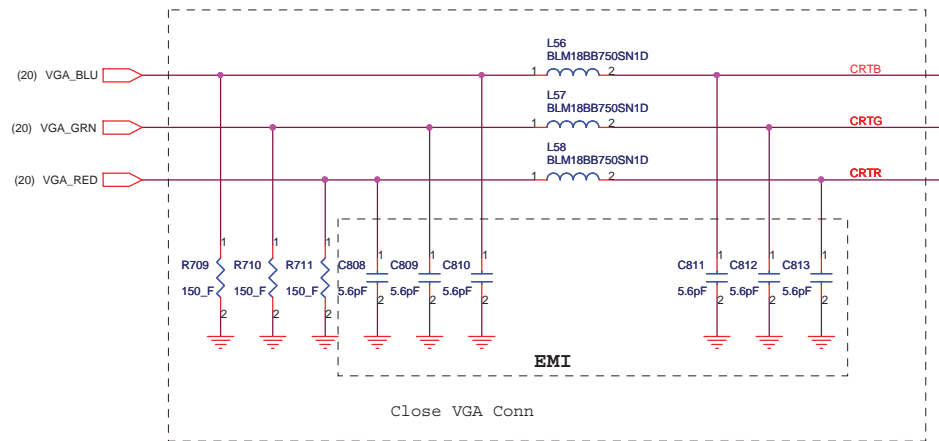
Title		
VGA-MXM-CON-2_A		
Size	Document Number	Rev
	Del/FLEX Confidential	A00
Date:	Thursday, March 12, 2009	Sheet 21 of 61



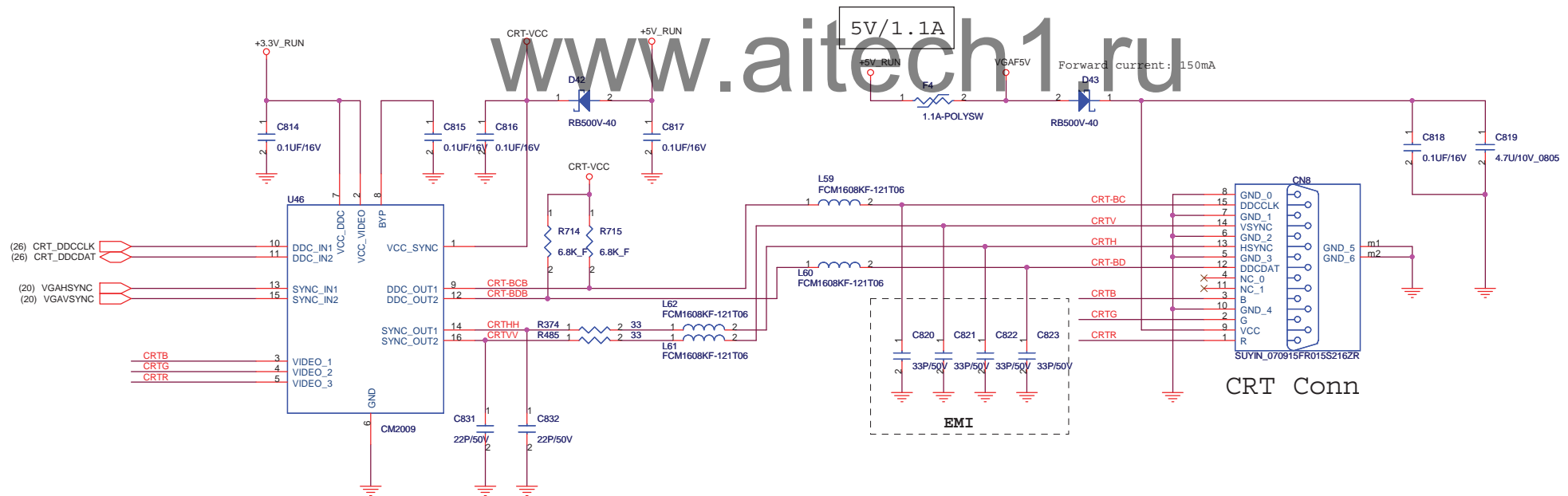


CONTROL BITS		I/O SELECTED	HOT PLUG DETECT STATUS	
S2	S1 (OEM)	Y/Z SCL_SINK SDA_SINK	HPD1	HPD2
H	H	SCL1 SDA1	HPD_SINK	L For NB-980T
H	L	SCL2 SDA2	L For NB-980TX	HPD_SINK



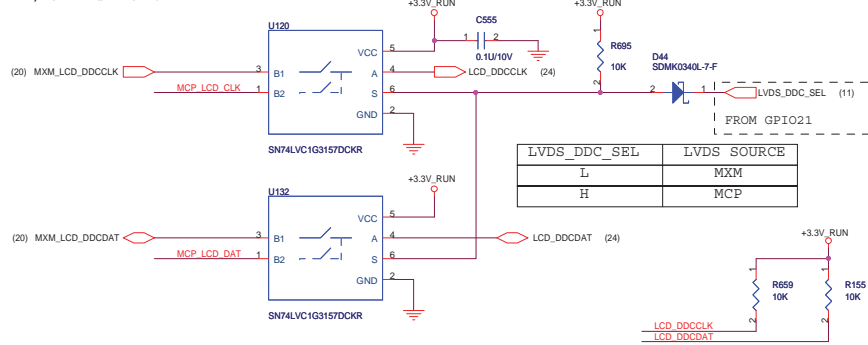


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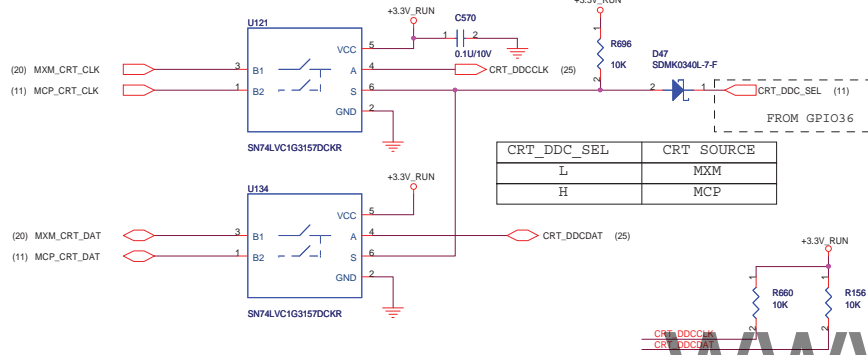


Title		
CRT CONN		
Size	Document Number	Rev
	DelI/FLEX Confidential	A00
Date:	Monday, March 09, 2009	Sheet 25 of 61

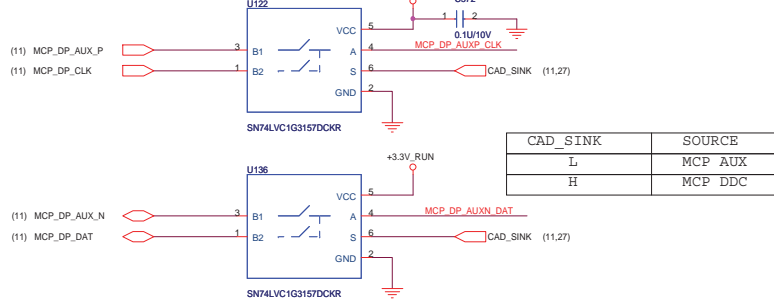
MXM/MCP LVDS DDC MUX



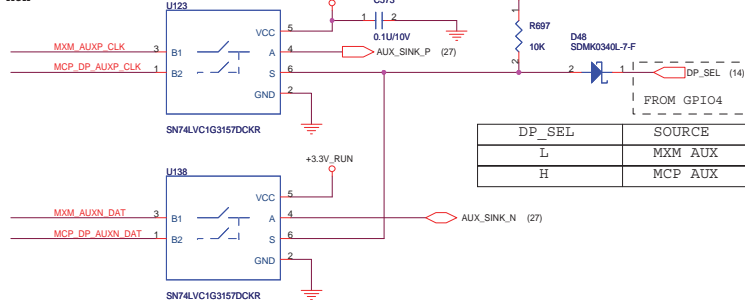
MXM/MCP VGA DDC MUX



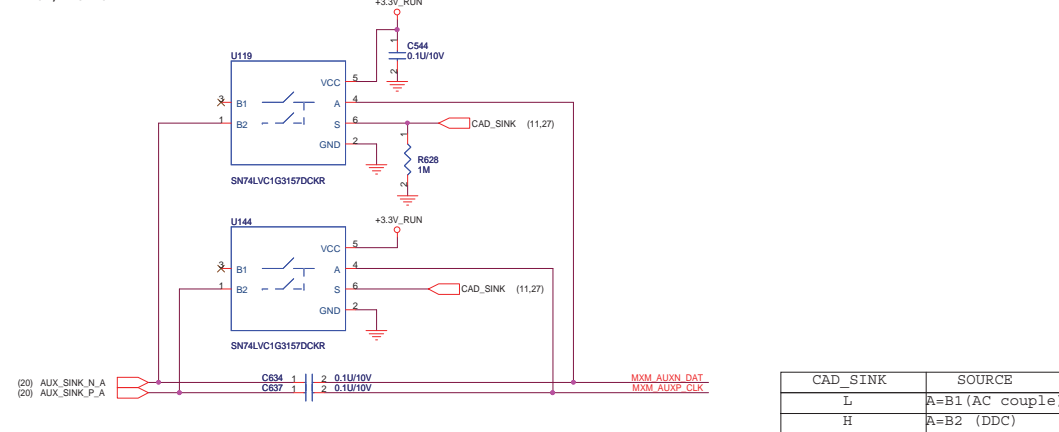
MCP AUX/DDC MUX



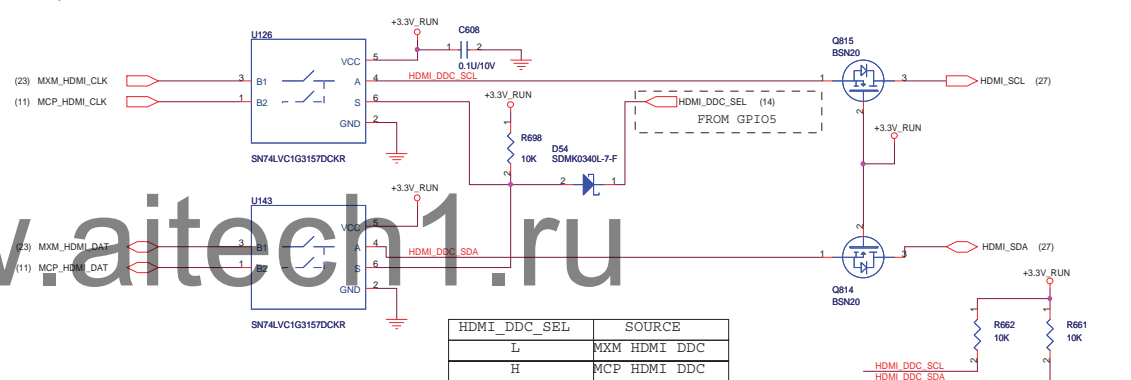
MXM/MCP DP AUX MUX



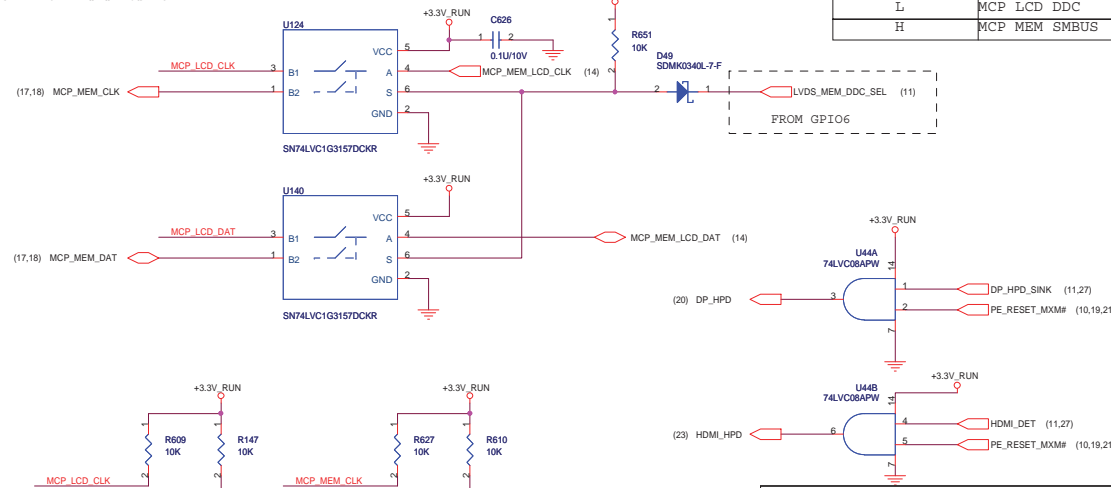
MXM DP AUX/DDC MUX



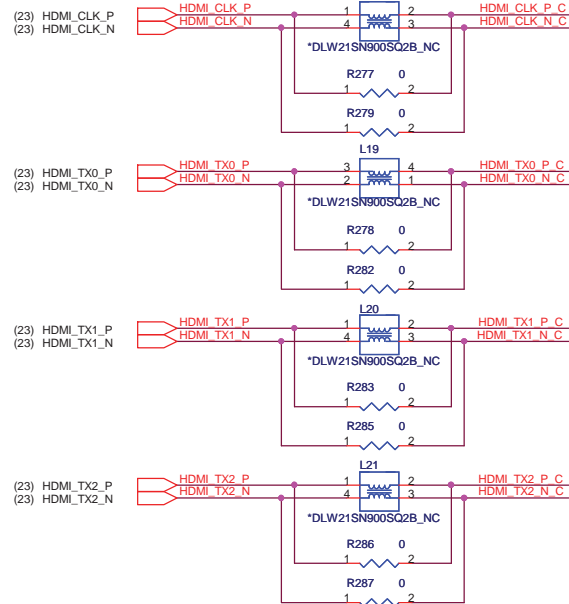
MXM/MCP HDMI DDC MUX



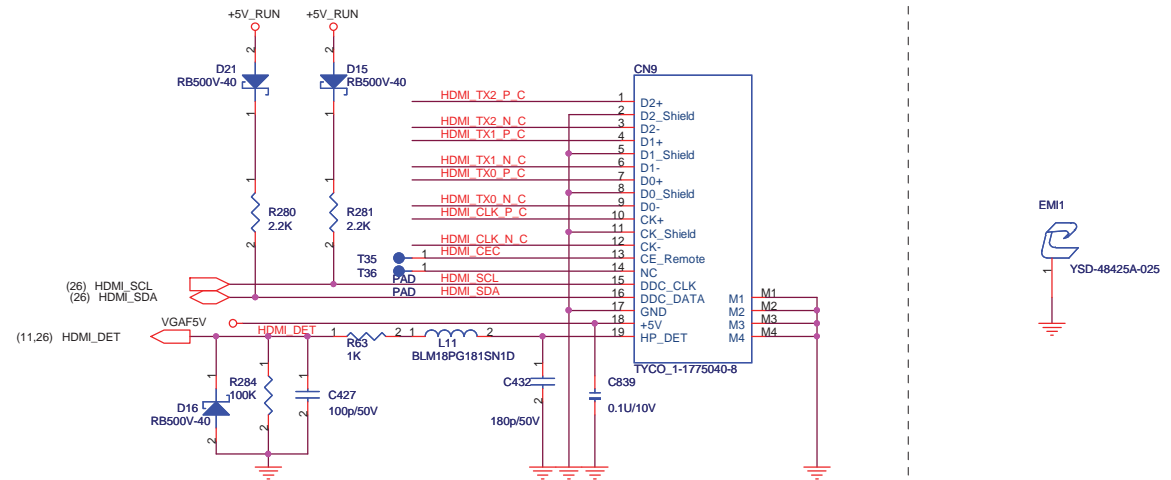
MCP MEM& LVDS SMBus MUX



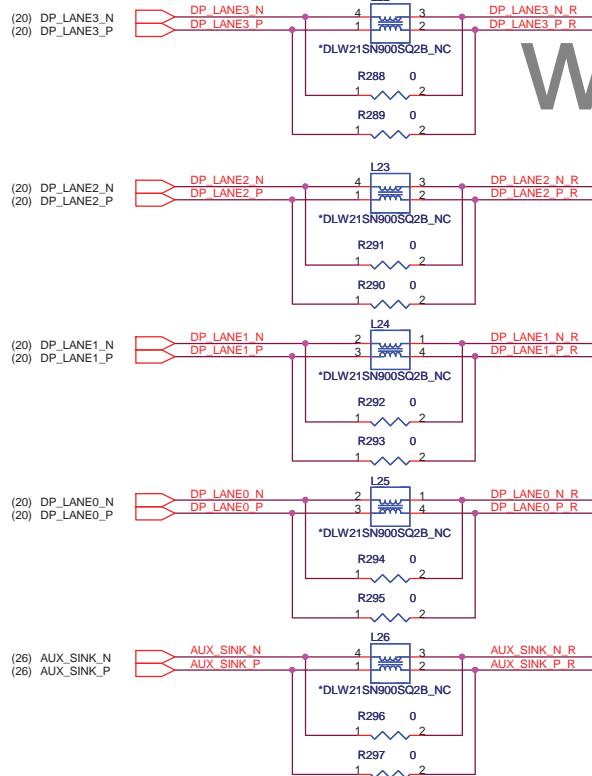
Reserve For EMI



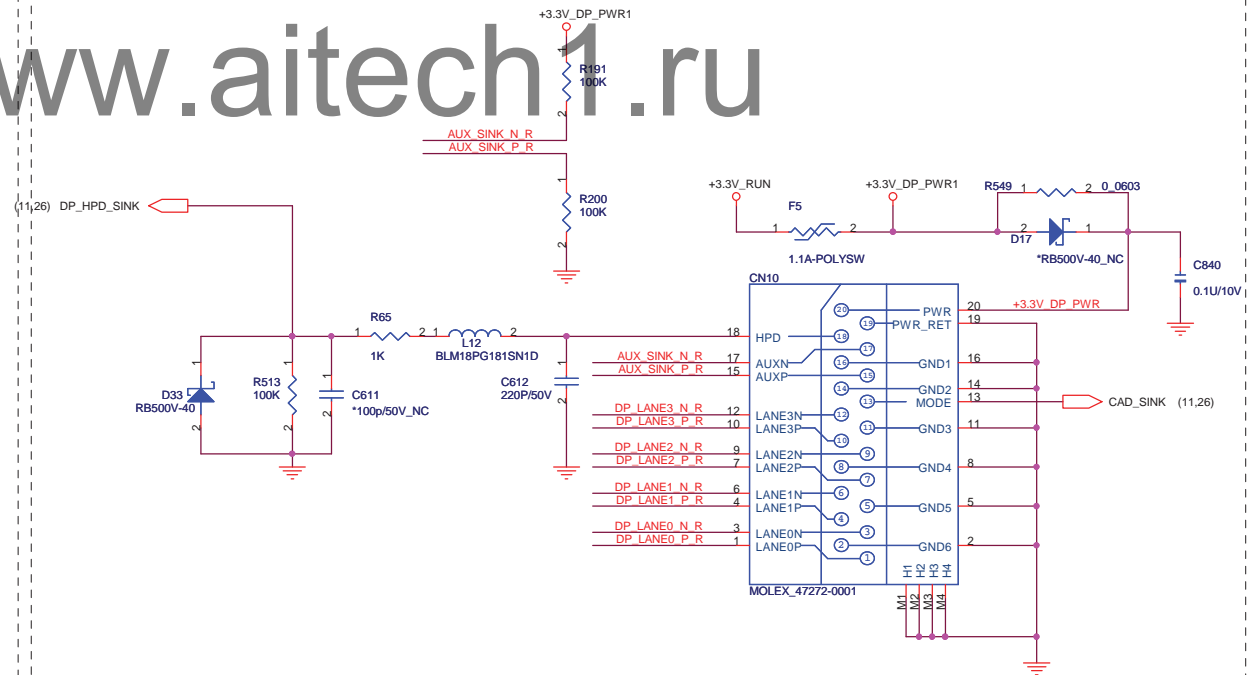
HDMI CONNECTOR



Reserve For EMI



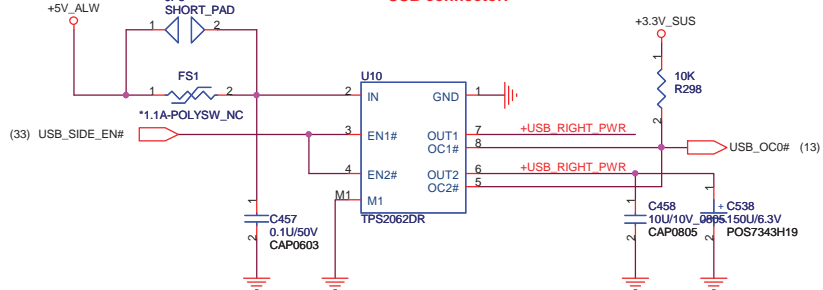
DISPLAY PORT CONNECTOR



Title		
HDMI & DP CONN		
Size	Document Number	Rev
	Del/FLEX Confidential	A00
Date:	Monday, March 09, 2009	Sheet 27 of 61

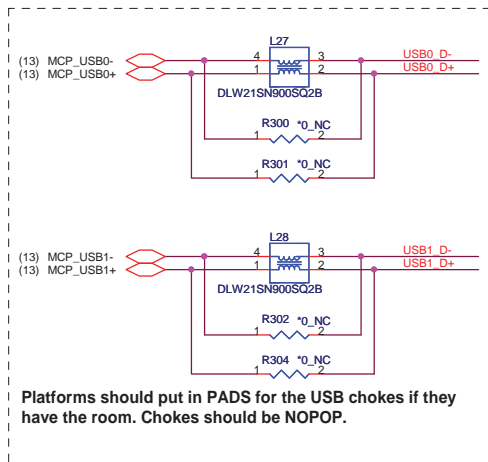
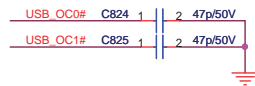
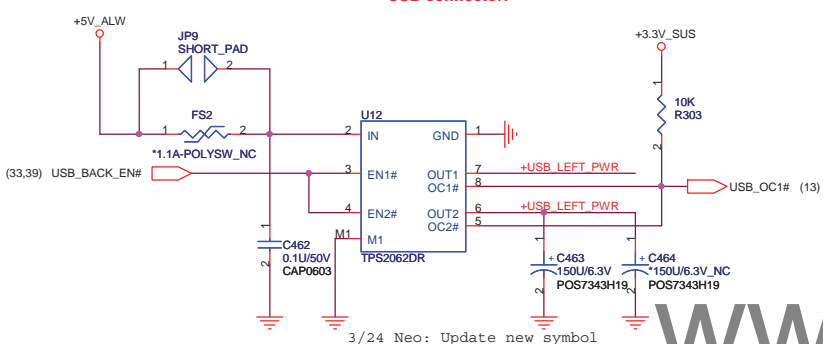
USB POWER SW

Place one 150uF cap by each USB connector.
Each channel is 1A

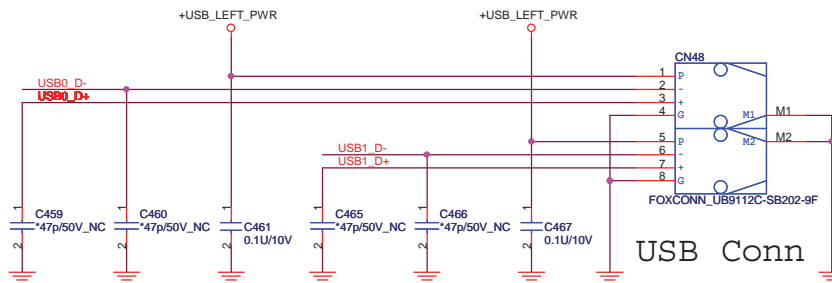


USB POWER SW

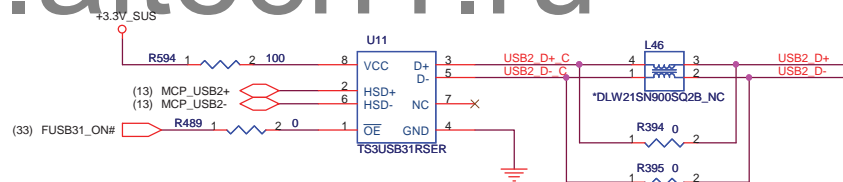
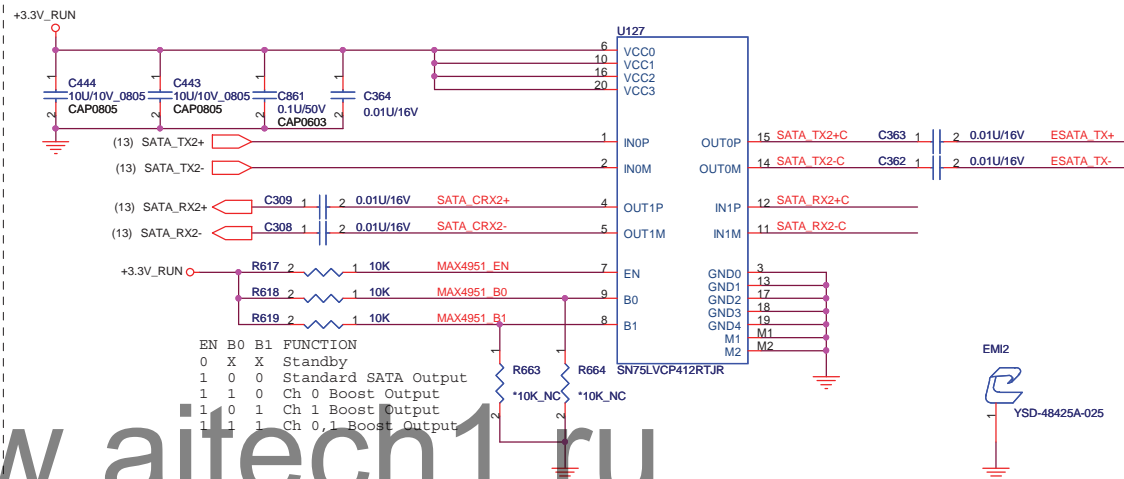
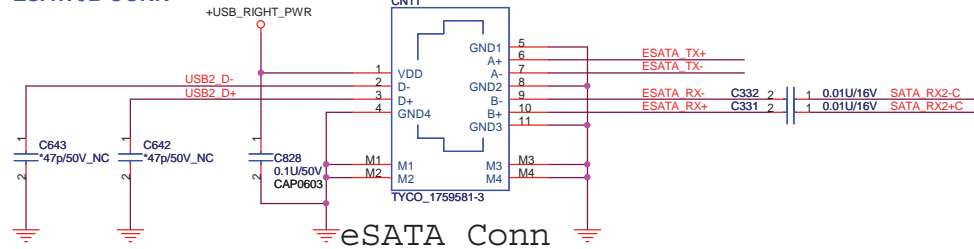
Place one 150uF cap by each USB connector.
Each channel is 1A



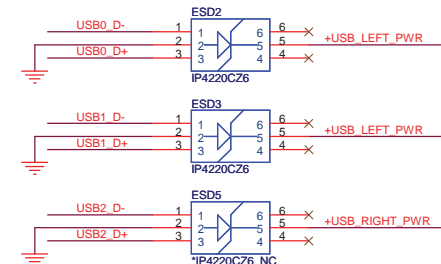
USB CONN

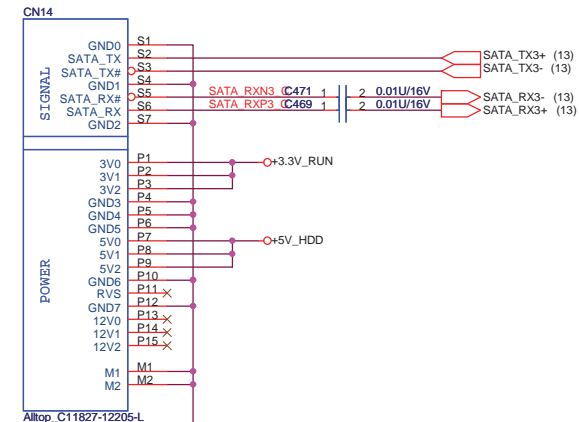


ESATA/B CONN



Place ESD diodes as close as USB connector.





Slave HDD Conn

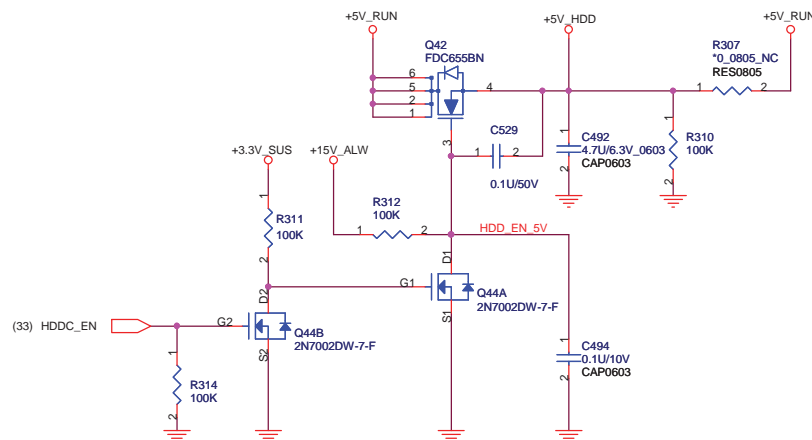
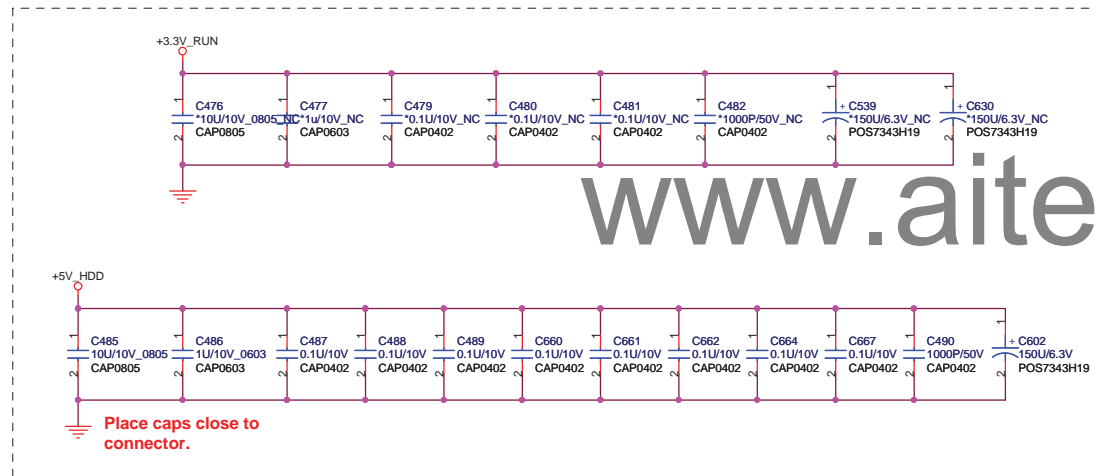
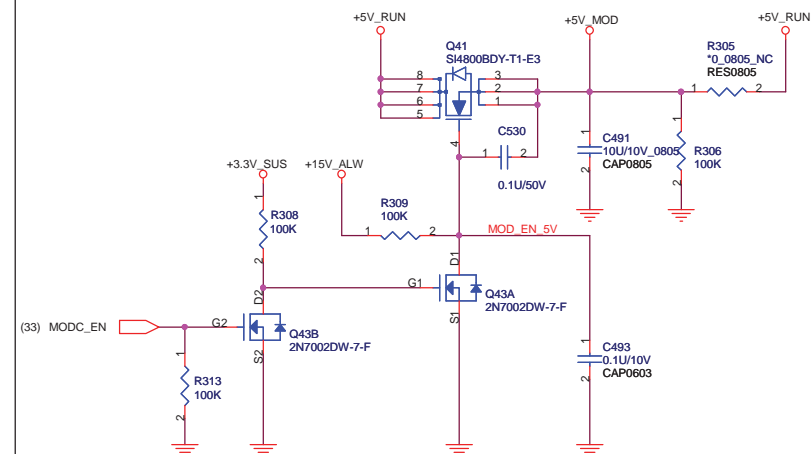
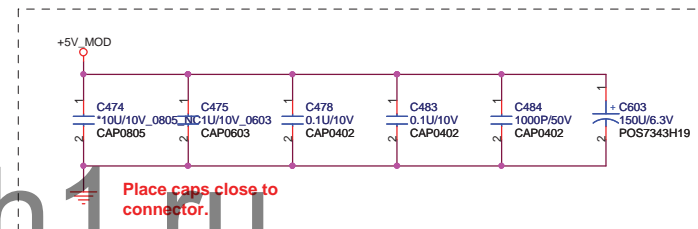
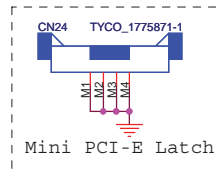


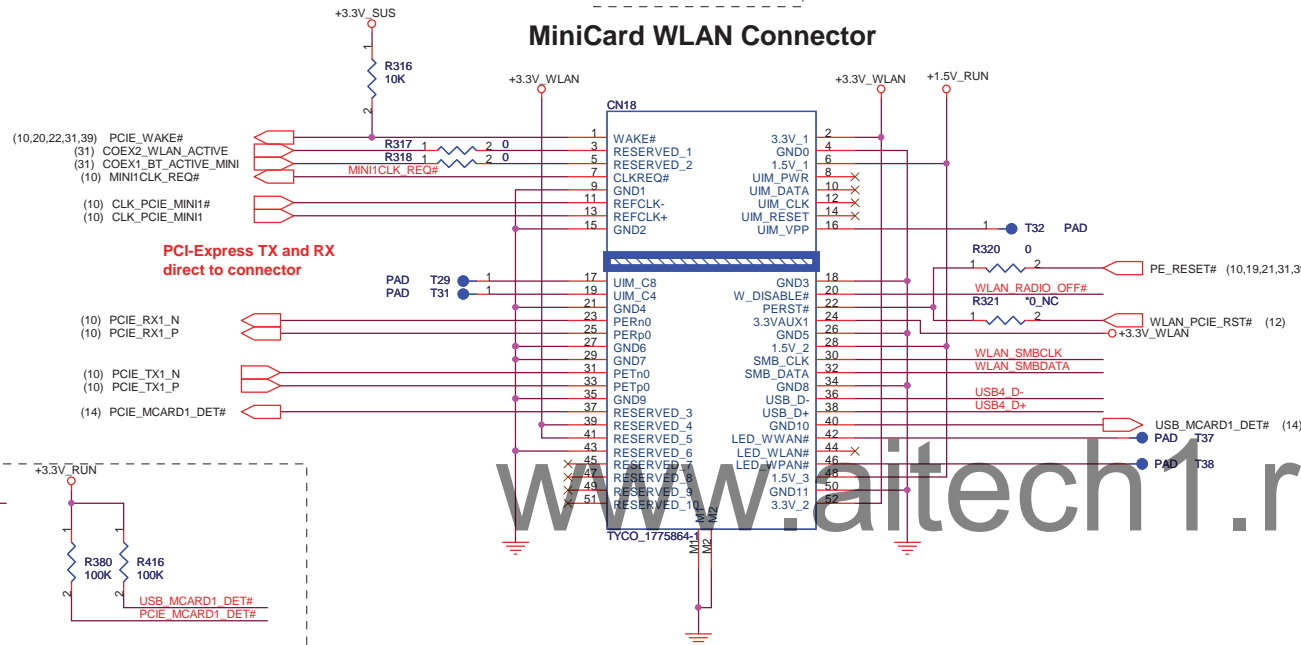
Diagram illustrating the pin connections for the HIROSE_FH28E-20S-0.5SH(11) connector. The connector is a 20-pin Hirose FH28E-20S-0.5SH(11) with pins labeled GND0, TXP, TXN, GND1, RXN, RXP, C_DEF#, NC0, NC1, NC2, GND2, GND3, GND4, GND5, GND6, +5V0, +5V1, +5V2, +5V3, +5V4, M1, and M2. The diagram shows connections to SATA signals: SATA_TX1+ (13) and SATA_TX1- (13) from TXP and TXN; SATA_RX1+ (13) and SATA_RX1- (13) from RXN and RXP; and ODD_CABLE_DET# (36) from C_DEF#. Power connections include +5V_MOD to +5V0 and +5V1, and M1 and M2 to ground. Signal labels include SATA_RXN1_C, SATA_RXP1_C, C473, and C472.

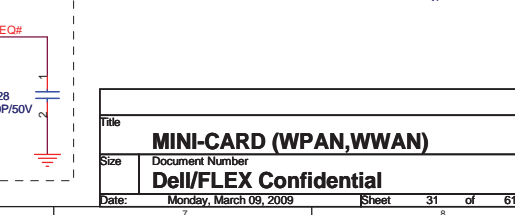
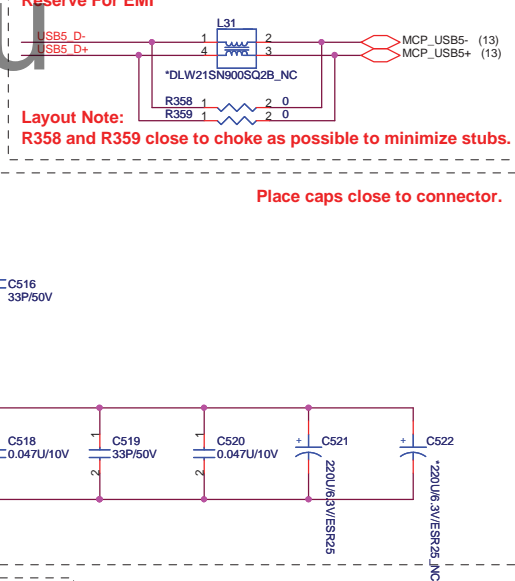
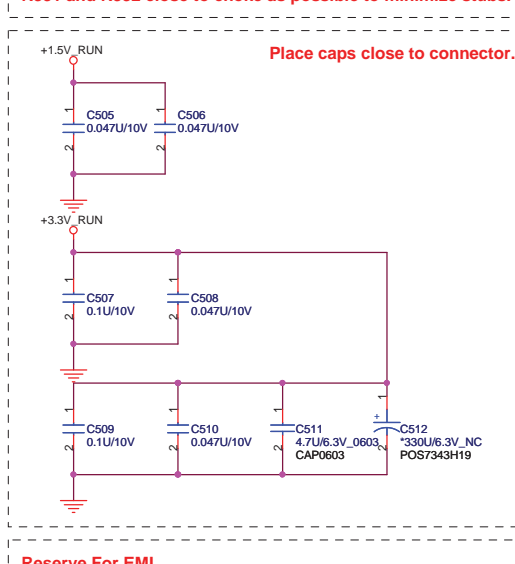
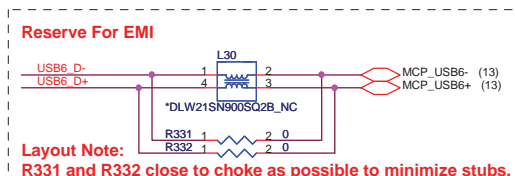
ODD Conn

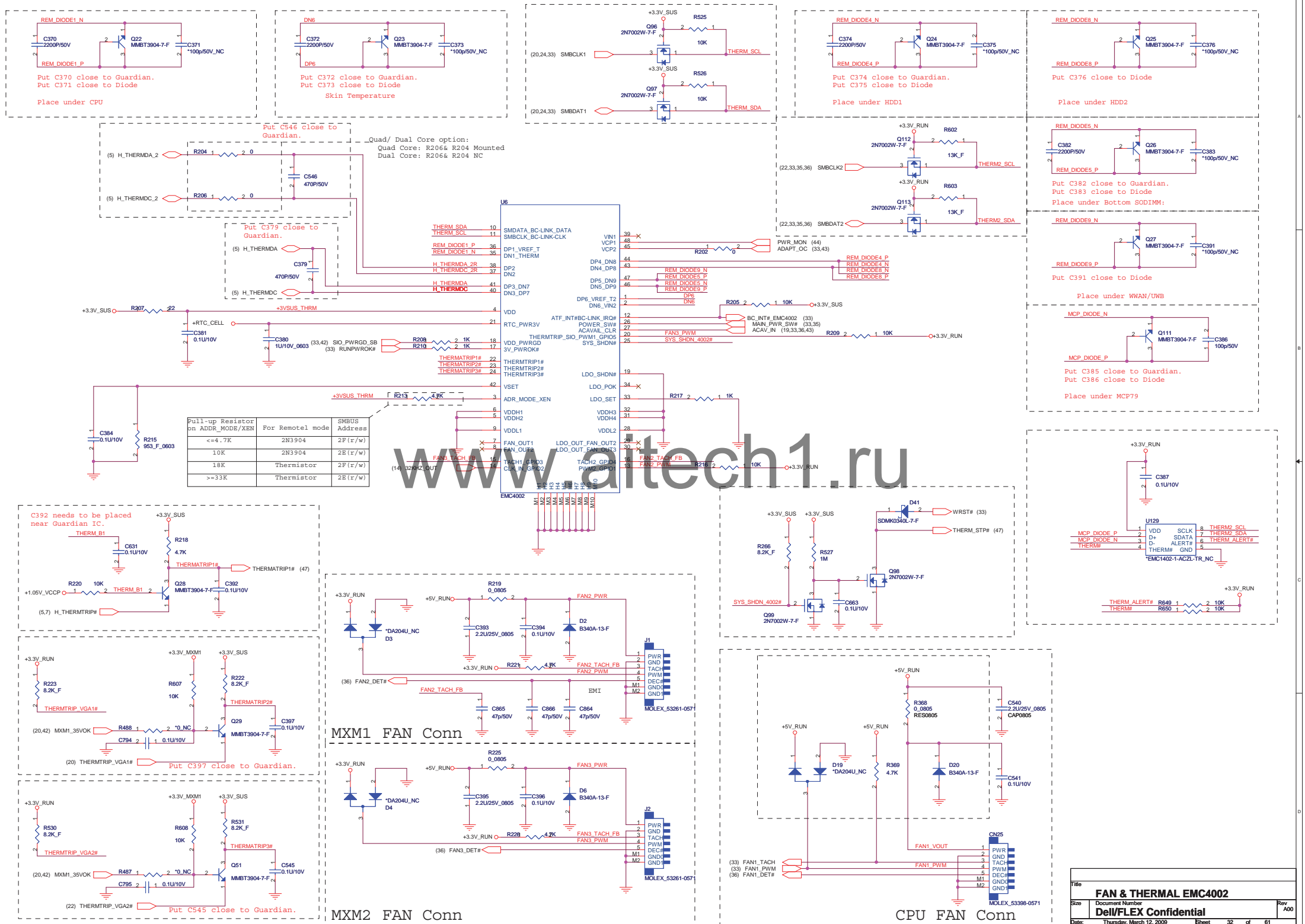




MiniCard WLAN Connector





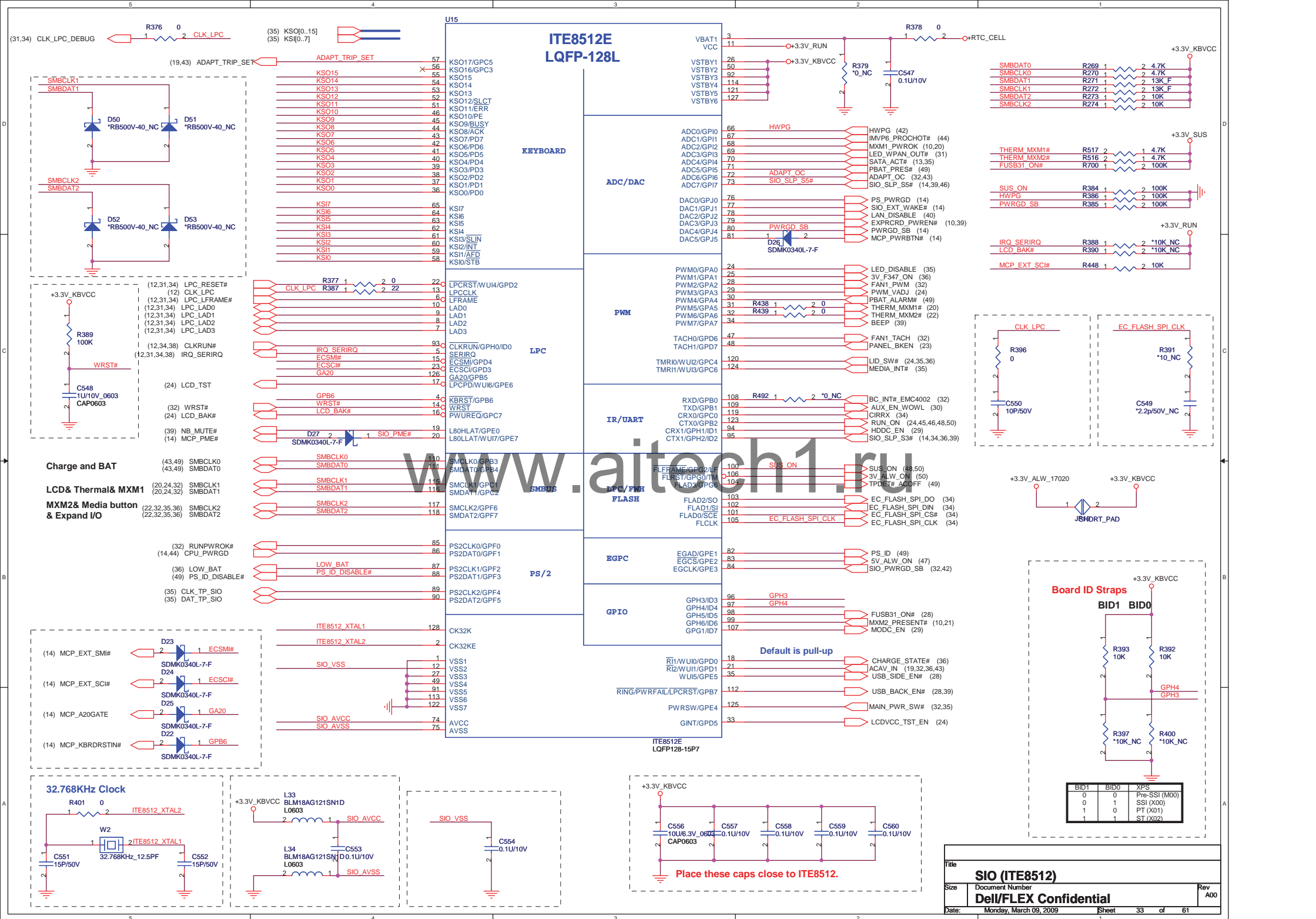


Pull-up Resistor on ADDR_MODE/XEN	For Remot mode	SMBUS Address
<=4.7K	2N3904	2F(r/w)
10K	2N3904	2E(r/w)
18K	Thermistor	2F(r/w)
>=33K	Thermistor	2E(r/w)

MXM1 FAN Conn

MXM2 FAN Conn

CPU FAN Conn



(33) EC_FLASH_SPI_CS#

(33) EC_FLASH_SPI_CLK

(33) EC_FLASH_SPI_DIN

(33) EC_FLASH_SPI_DO

R407 1 2 15

R405 1 2 15

R404 1 2 15

+3.3V_KBVCC

R403 10K

U17

CE# 1

SCK 6

SI 5

SO 2

HOLD# 7

WP# 3

VDD 8

VSS 4

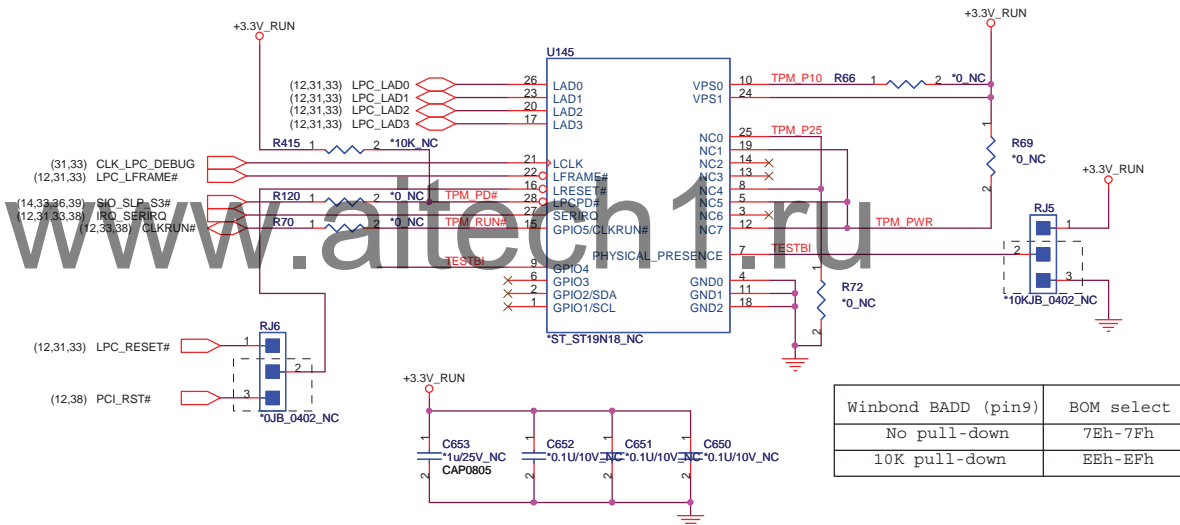
SST25VF016B-50-4C-S2AF

+3.3V_KBVCC

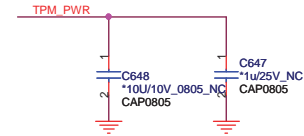
R406 10K

C563 22p/50V

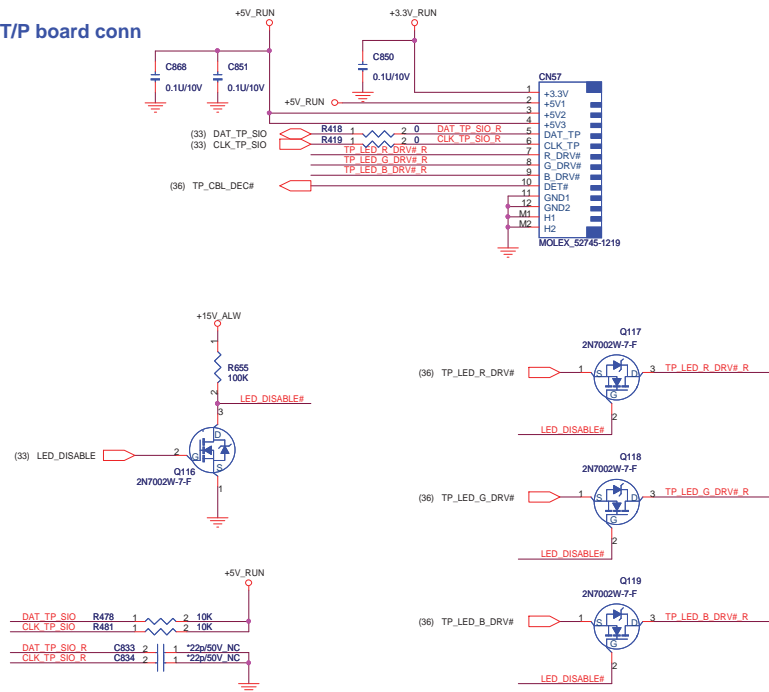
C564 0.1u/10V



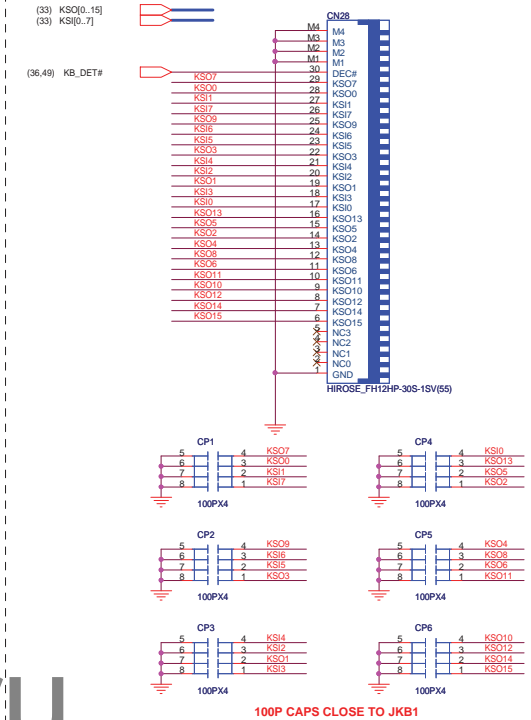
TPM Vendor	BOM select
ST	Mounted: R66 NA: R69, R70, R72, C647, C648
Winbond	NA: R66 Mounted: R69, R70, R72, C647, C648



T/P board conn

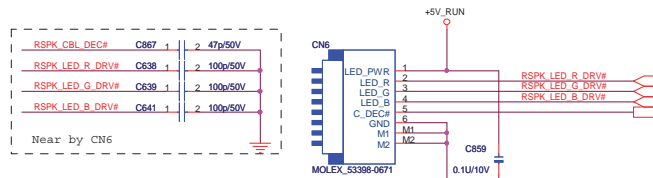


KEYBOARD CONNECTOR

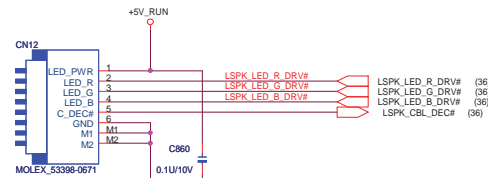


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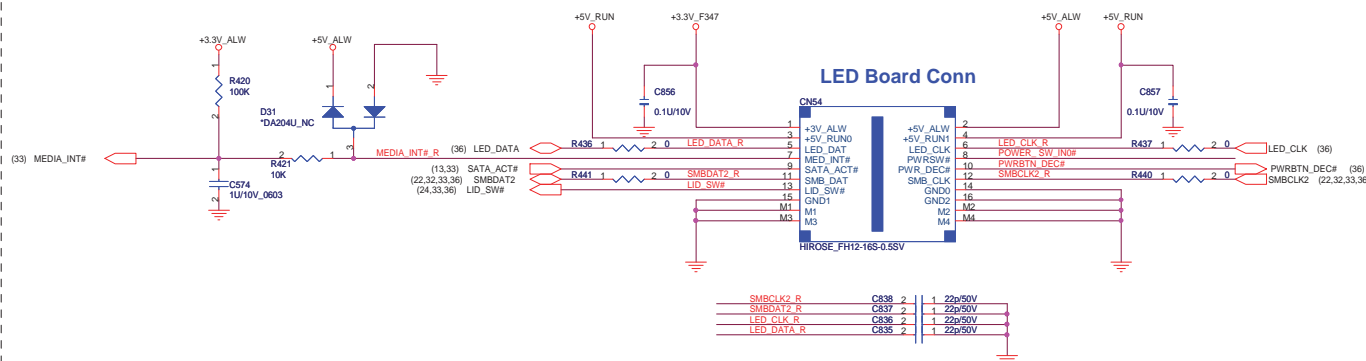
Right SPK LED Conn



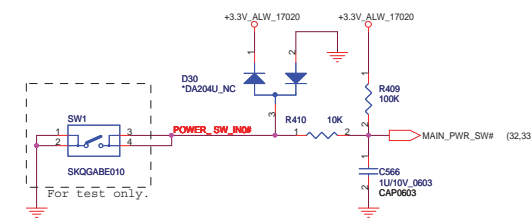
Left SPK LED Conn

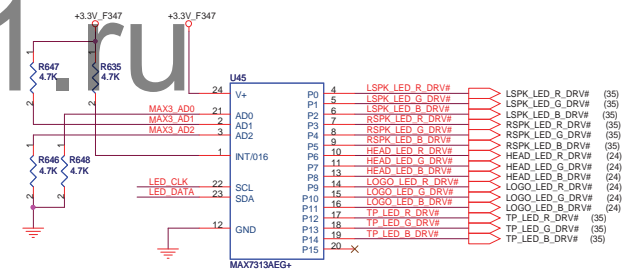
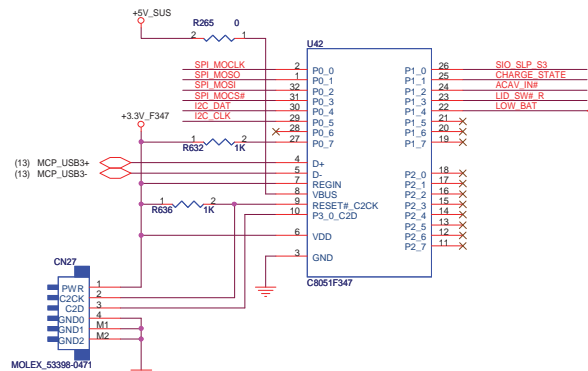
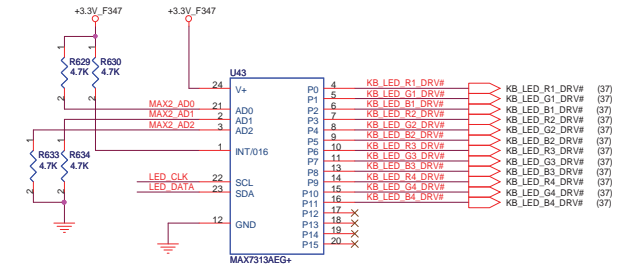
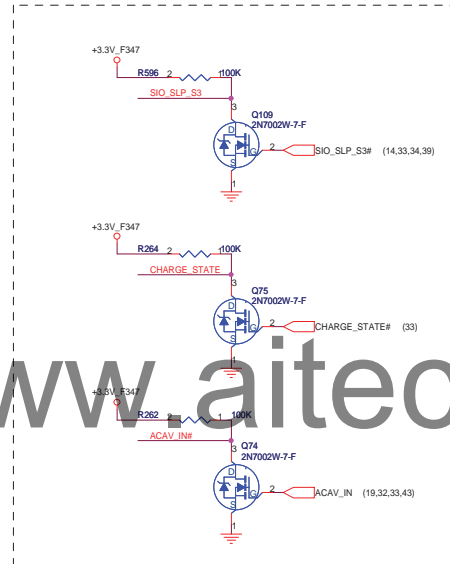
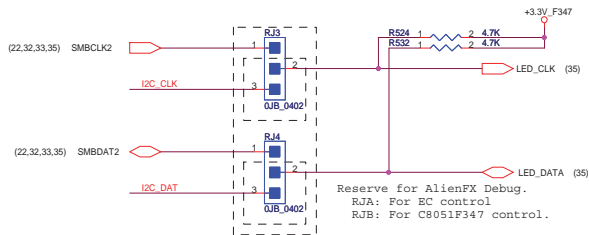
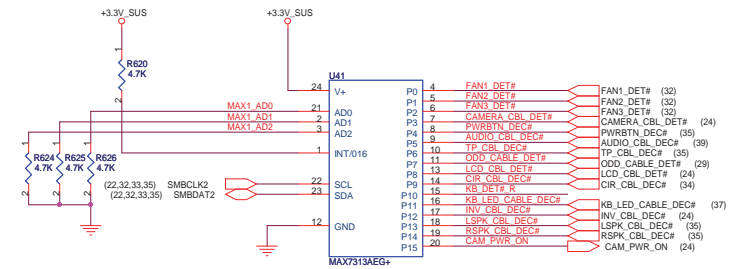
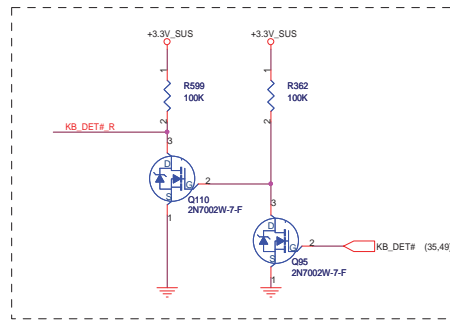
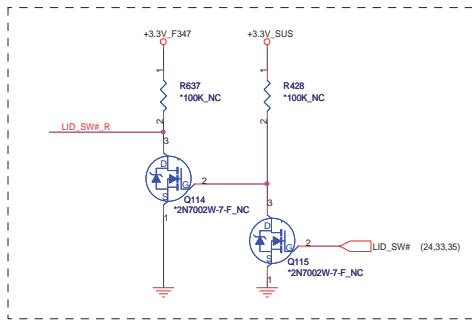


LED Board Conn



Power Button

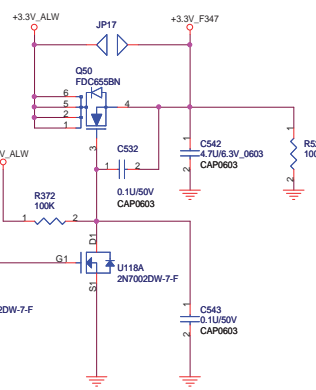




+3.3V_F347 behavior

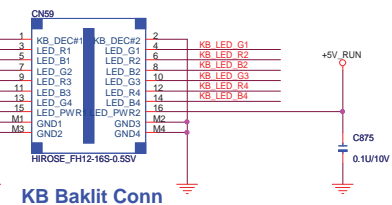
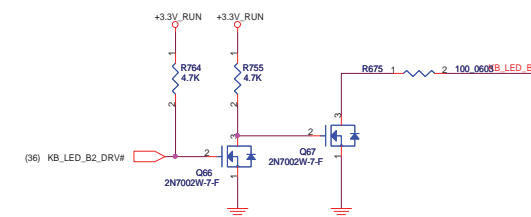
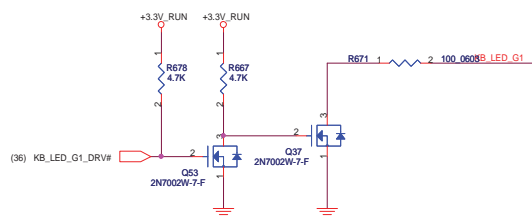
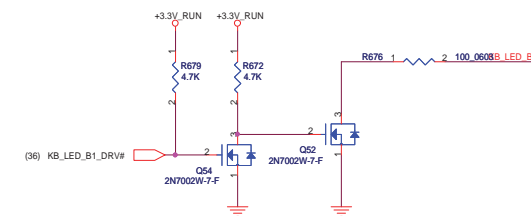
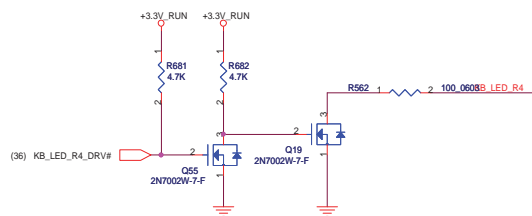
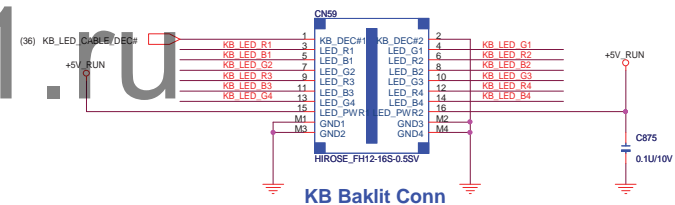
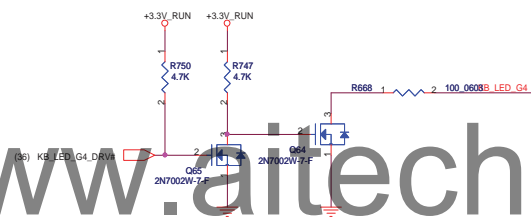
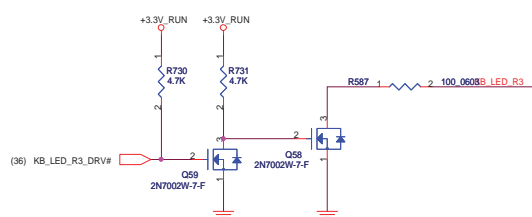
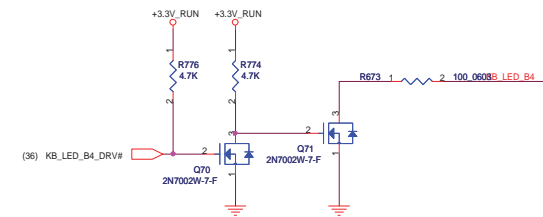
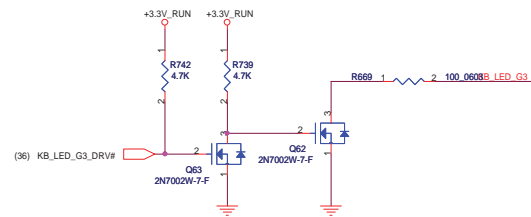
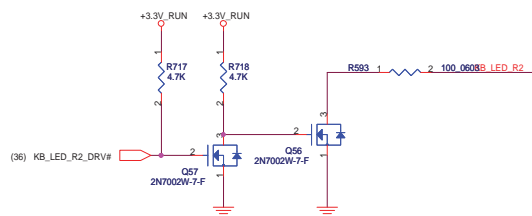
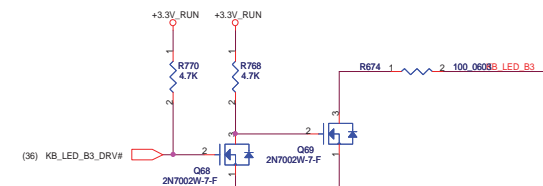
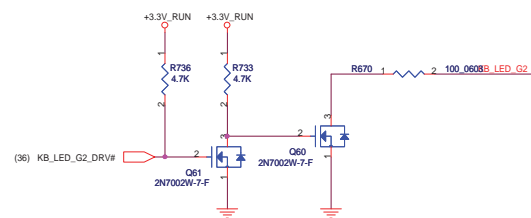
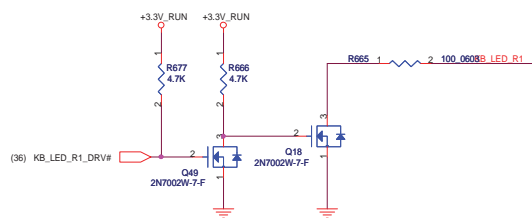
	State				
	S0	S3	S4	S5	
AC In	ON	ON	ON	ON	
BAT only	ON	ON	Off	Off	

AC mode Battery full in S5;
turn off ELC controller.

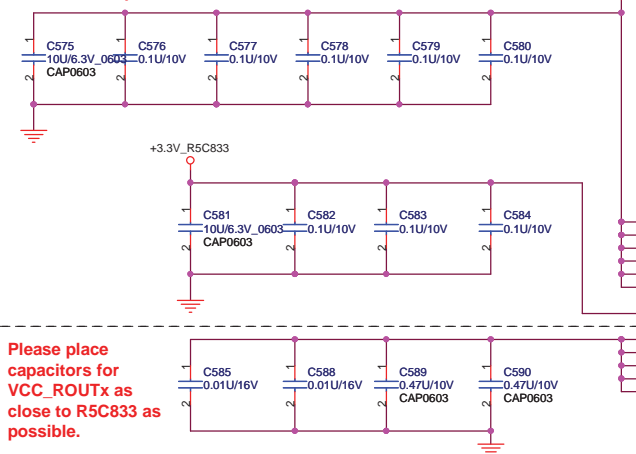


Reference	AD2	AD1	AD0	MAX7313 #
U41	0	0	0	Cable Detect#
U43	0	0	1	KB LED
U45	0	1	0	SPK& Head& Logo& T/P LED
---	0	1	1	LED Board
---	1	0	0	Media Board
---	1	0	1	Media Board

CAMERA_CBL_DET#	R427	1	2	100K
AUDIO_CBL_DEC#	R431	1	2	100K
TP_CBL_DEC#	R445	1	2	100K
ODD_CABLE_DET#	R446	1	2	100K
LCD_CBL_DET#	R447	1	2	100K
CIR_CBL_DEC#	R450	1	2	100K
KB_LED_CABLE_DEC#	R475	1	2	100K
FAN1_DET#	R462	1	2	100K
FAN2_DET#	R476	1	2	100K
FAN3_DET#	R477	1	2	100K
INV_CBL_DEC#	R480	1	2	100K
LSPK_CBL_DEC#	R483	1	2	100K
RSPK_CBL_DEC#	R484	1	2	100K
PWRBTN_DEC#	R680	1	2	100K
CAM_PWR_ON	R687	1	2	100K

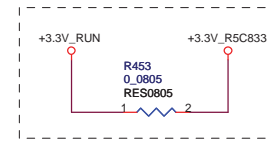


Place the power caps close to the relation pins.

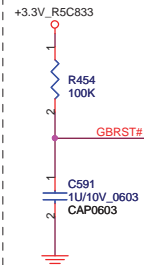
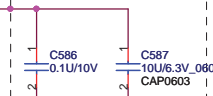


Please place capacitors for VCC_ROUTx as close to R5C833 as possible.

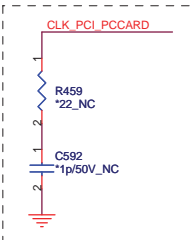
(12) PCI_AD[31..0]



Place the power caps close to the relation pins.



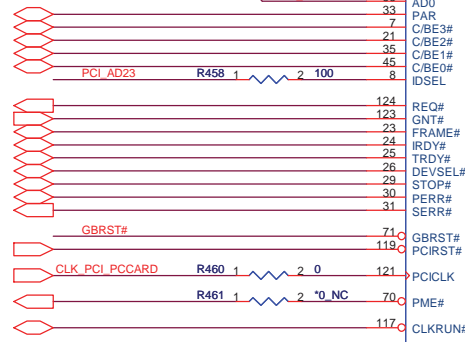
GBRST# should be asserted only when system power supply is on.



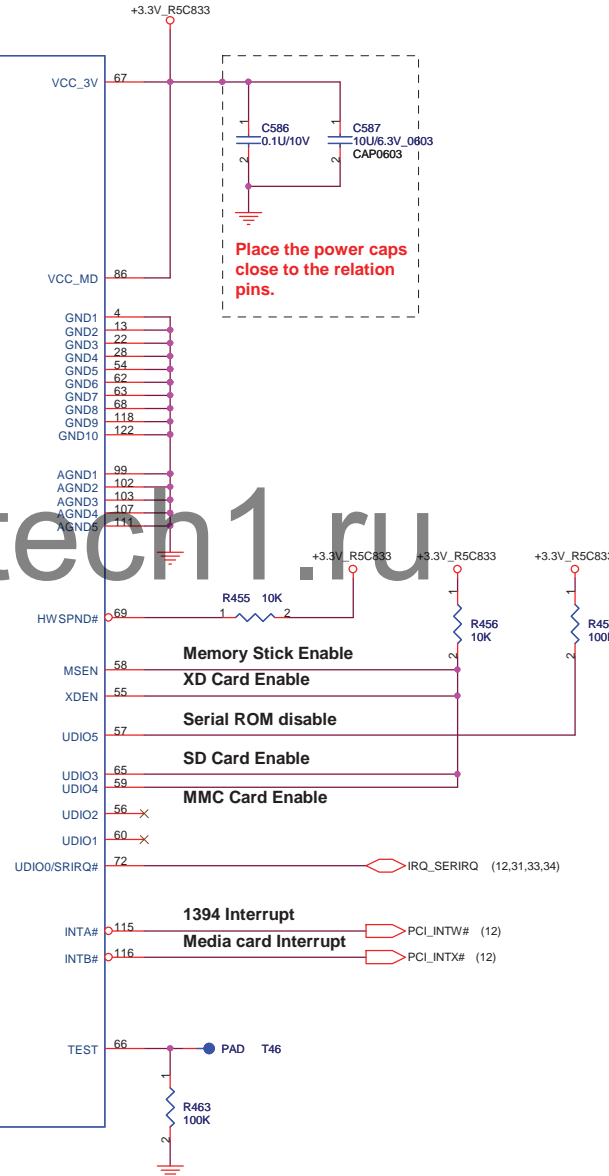
(12) PCI_PAR
(12) PCI_C_BE3#
(12) PCI_C_BE2#
(12) PCI_C_BE1#
(12) PCI_C_BE0#

(12) PCI_REQ0#
(12) PCI_GNT0#
(12) PCI_FRAME#
(12) PCI_IRDY#
(12) PCI_TRDY#
(12) PCI_DEVSEL#
(12) PCI_STOP#
(12) PCI_PERR#
(12) PCI_SERR#

(12,34) PCI_RST#
(12) CLK_PCI_PCCARD
(12) PCI_PME#
(12,33,34) CLKRUN#



PCI / OTHER



Memory Stick Enable

XD Card Enable

Serial ROM disable

SD Card Enable

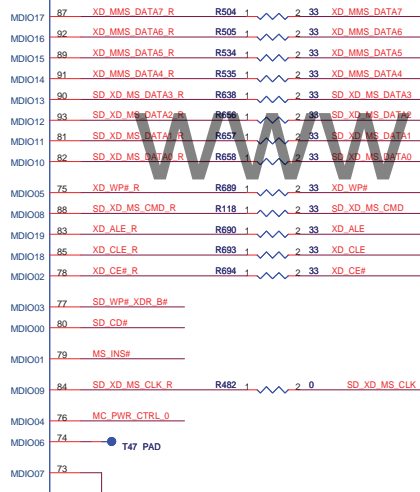
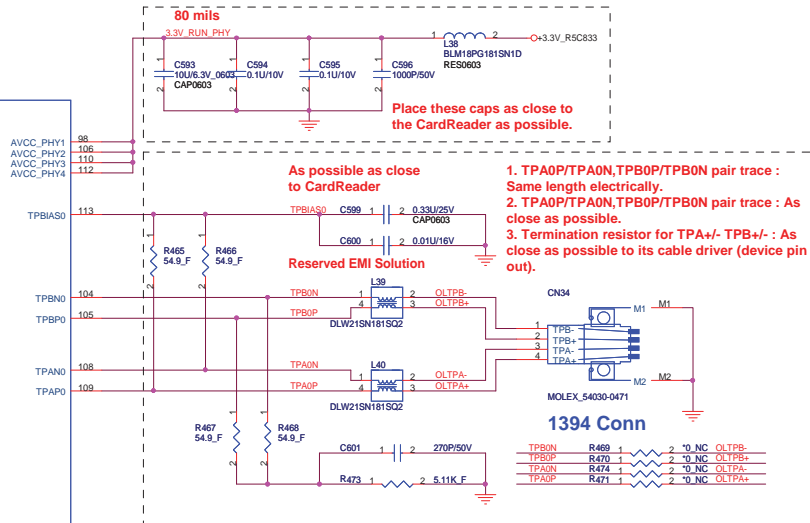
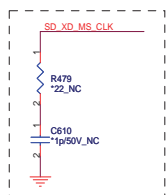
MMC Card Enable

1394 Interrupt

Media card Interrupt

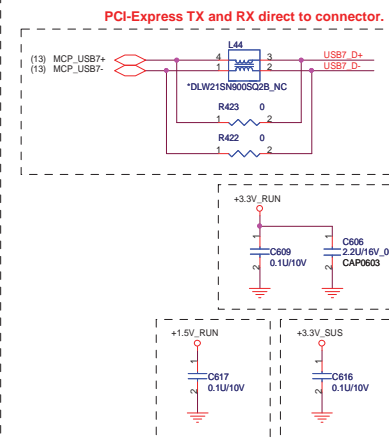
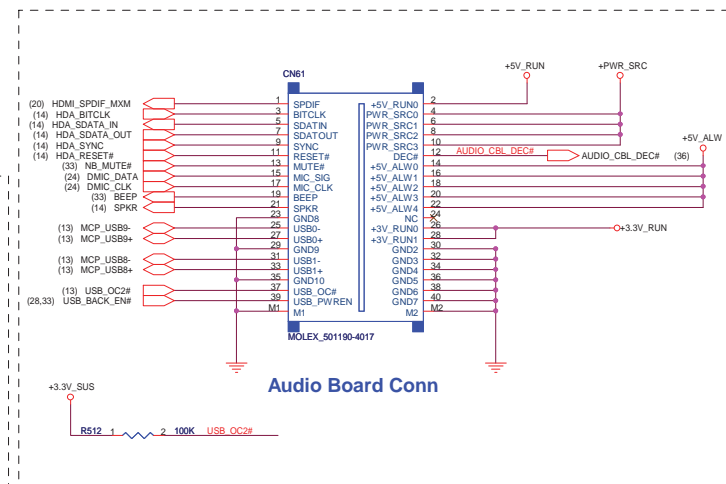
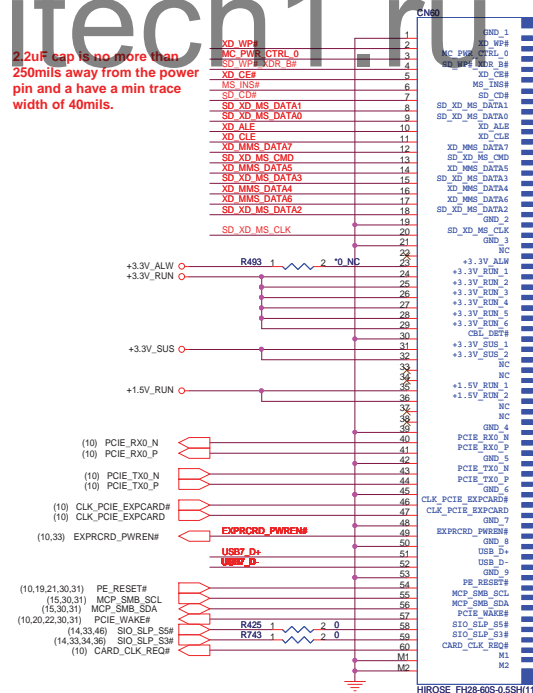
PCI_INTW# (12)

PCI_INTX# (12)



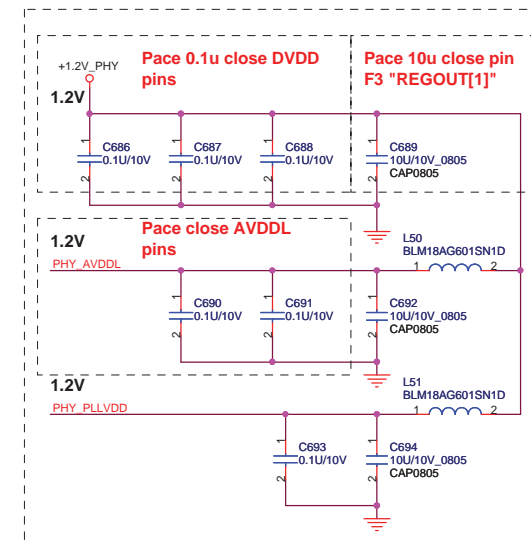
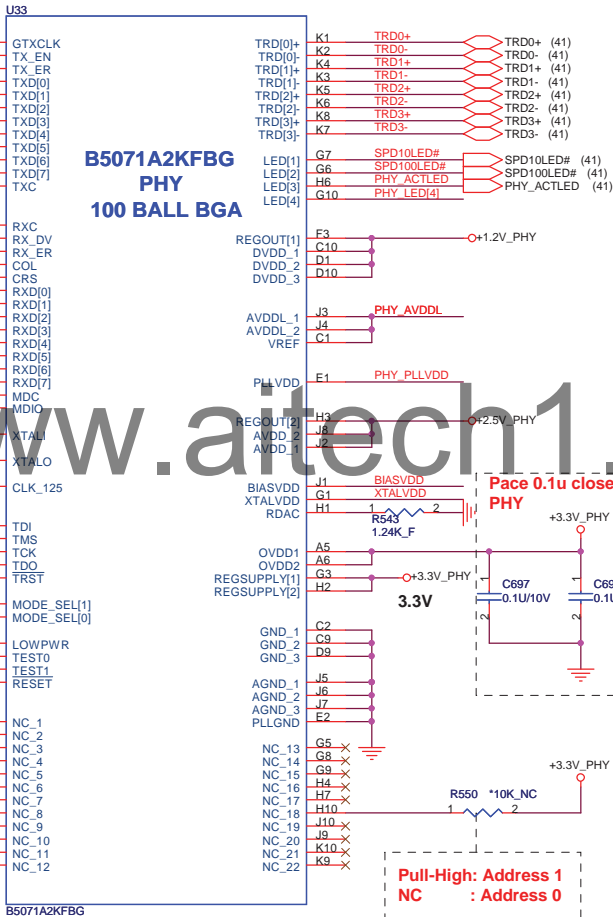
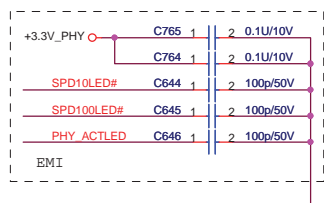
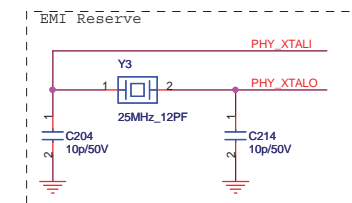
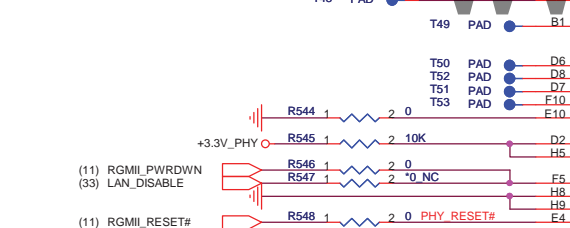
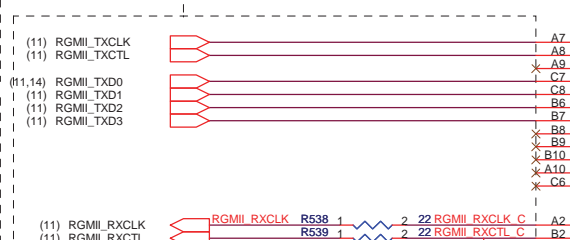
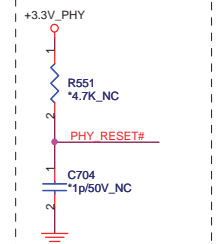
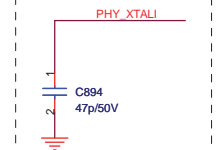
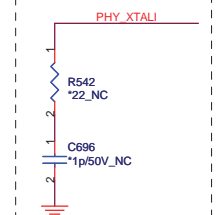
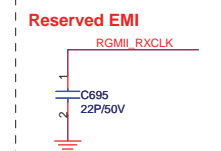
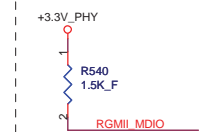
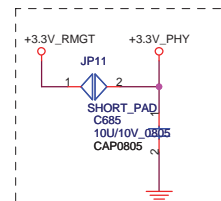
Express Card Conn

2.2uF cap is no more than 250mils away from the power pin and a have a min trace width of 40mils.

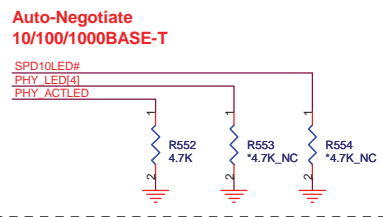
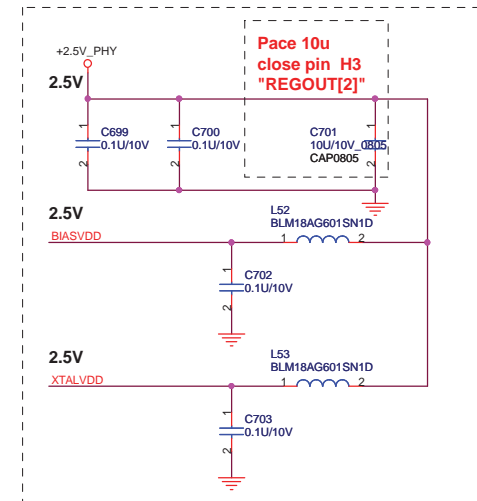


Layout Note:

1. Use 50 ohm impedance for all trace.
2. Trace length matched to a tolerance of 9.8mm in order to keep the skew between signals less than 0.07ns.
3. The receive and transmit signals kept away from each other and other analog and clock signals to reduce crosstalk.



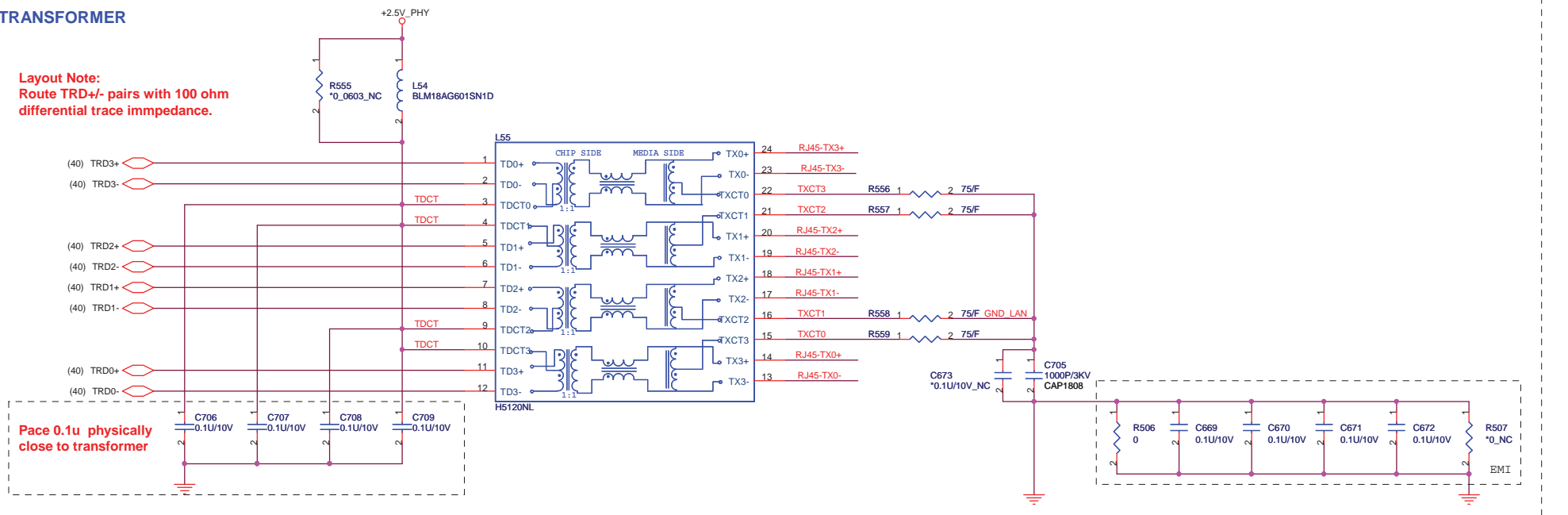
Layout Note:
Locate the RDAC resistor as close to the RDAC pin as possible and keep the trace between the pin and resistor and short and wide as possible.



Title			
PHY(B5071)			
Size	Document Number		Rev
	Del/FLEX Confidential		A00
Date:	Thursday, March 12, 2009	Sheet	40 of 61

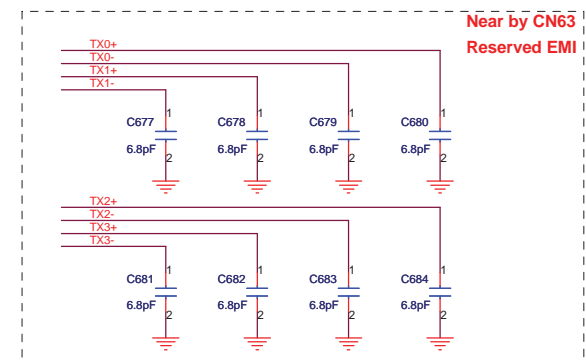
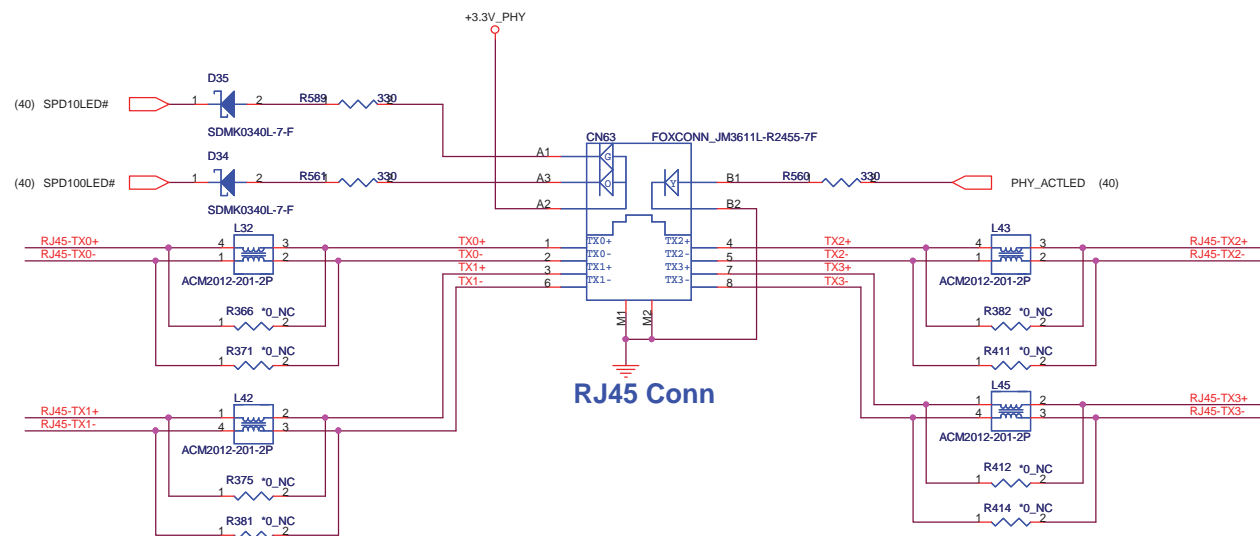
TRANSFORMER

Layout Note:
Route TRD+/- pairs with 100 ohm differential trace impedance.

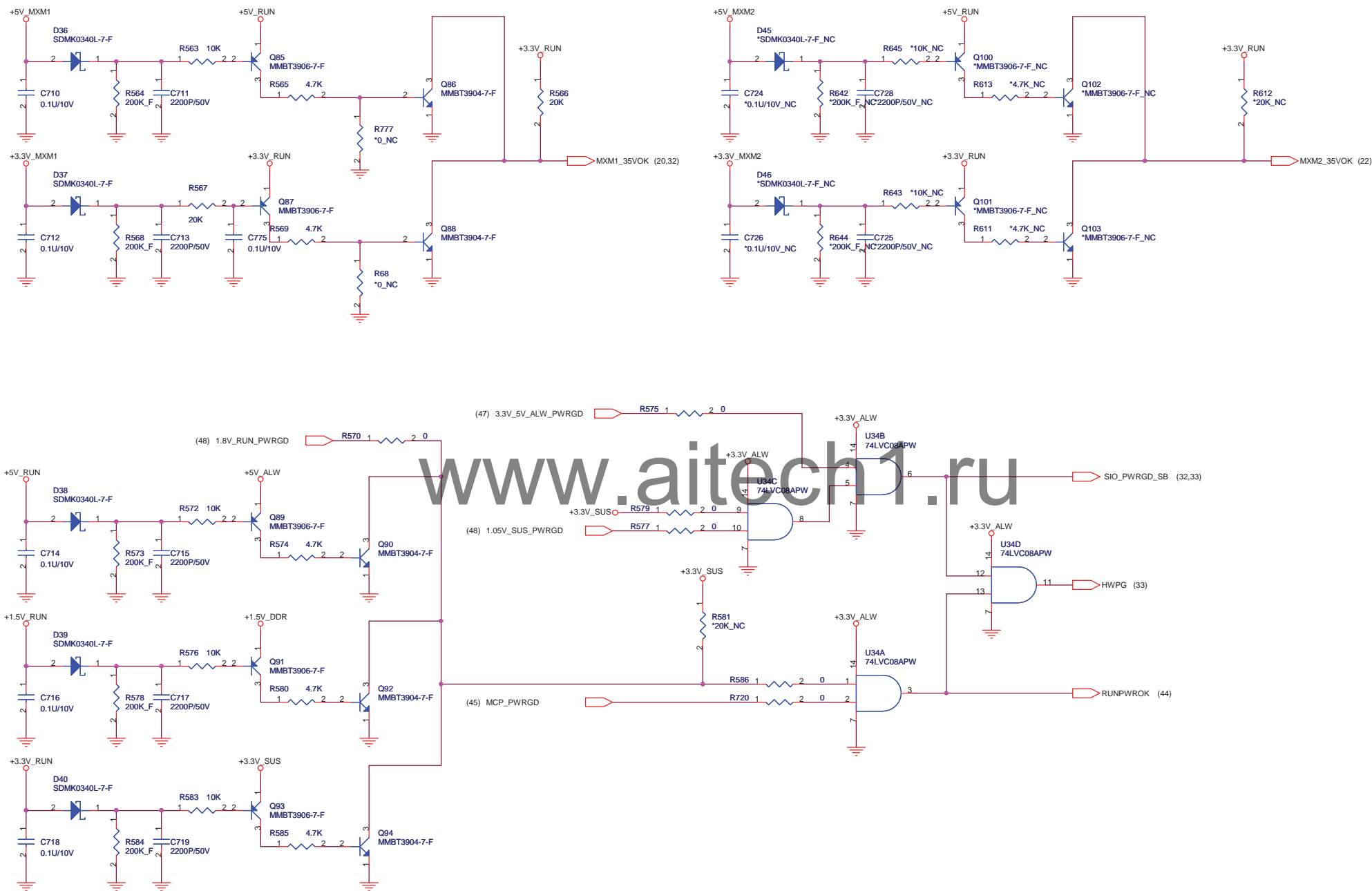


RJ-45 Connector

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Title			
RJ-45/TRANSFORM			
Size	Document Number		Rev
	Del/FLEX Confidential		A00
Date:	Thursday, March 12, 2009	Sheet	41 of 61



Title		
System Reset Circuit		
Size	Document Number	Rev
	Dell/FLEX Confidential	A00
Date:	Thursday, March 12, 2009	Sheet 42 of 61

Note:
Component Values on Schematic are for MAX8731 only.
Please see table 1-3 for BQ24745 or ISL88731
component Values.

TABLE 3. PIN NAME DIFFERENCES			
PIN	MAX8731A	ISL88731	bq24745
1	GND	NC	ICREF
3	REF	VREF	VREF
4	CCS	ICOMP	EAO
5	CCI	NC	EAI
6	CCV	VCOMP	FBO
7	DAC	NC	CE
8	IINP	ICM	VICM
11	VDD	VDDSMB	VDDSMB
14	BATSEL	NC	NC
15	FBSA	VFB	VFB
16	FBSB	NC	NC
17	CSIN	CSIN	CSIN
18	CSIP	CSOP	CSOP
20	DLO	LAGTE	LAGTE
21	LDO	VDDP	VDDP
23	LX	PHASE	PHASE
24	DHI	UGATE	UGATE
26	BST	BOOT	BOOT
25	VCC	VCC	ICOUT

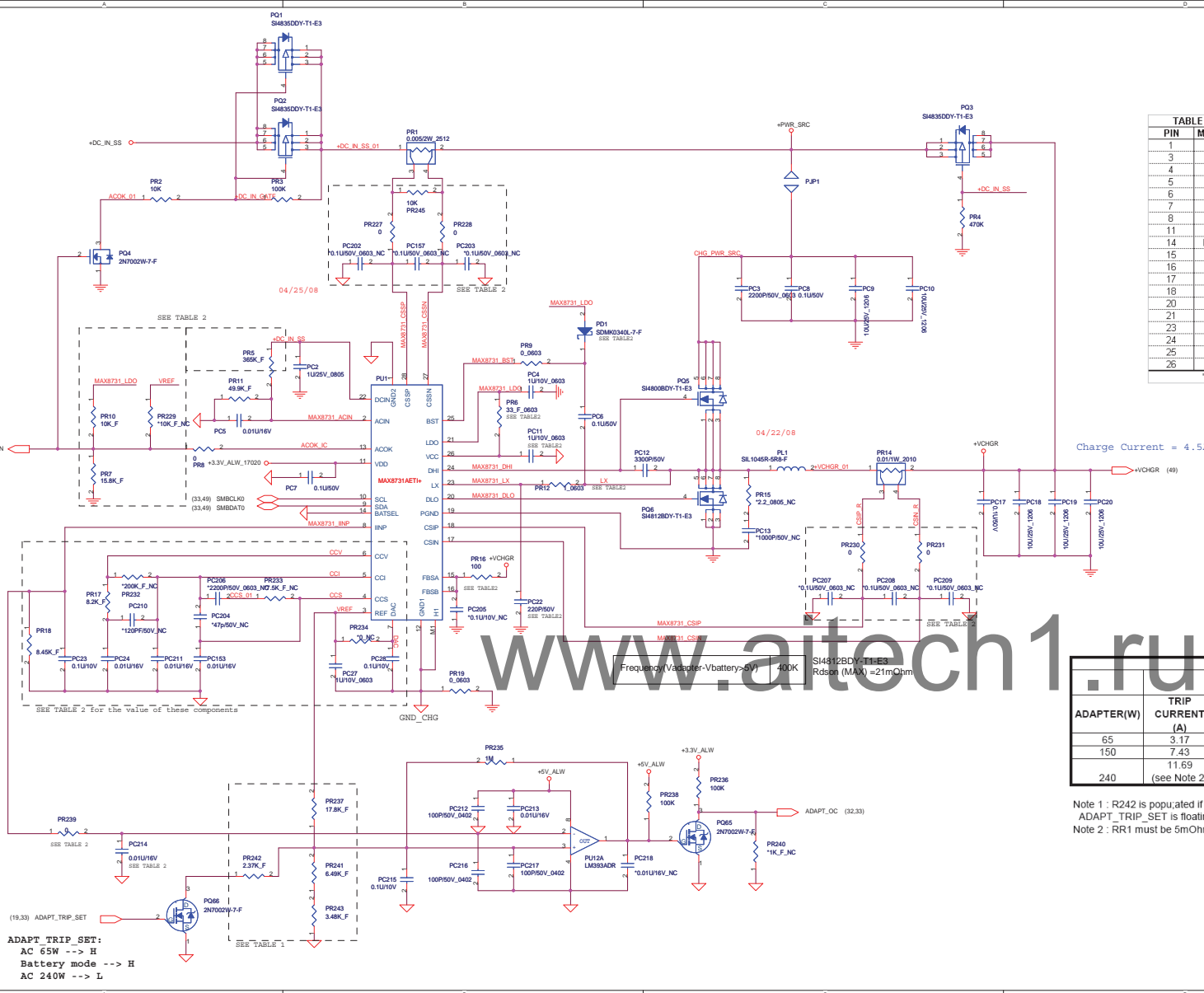
"NC" means no-connect

TABLE 2 BOM DIFFERENCES			
REF DES	MAXIM	INTERSIL	TI
PR245	NO STUFF	10K, 0.402, 5%	NO STUFF
PR227	0.0402, 5%	10, 0.402, 5%	0.0402, 5%
PR228	0.0402, 5%	10, 0.402, 5%	0.0402, 5%
PC157	NO STUFF	0.1uF	0.1uF
PC202	NO STUFF	NO STUFF	0.1uF
PC203	NO STUFF	NO STUFF	NO STUFF
PR230	0.0402, 5%	10, 0.402, 5%	0.0402, 5%
PR231	0.0402, 5%	10, 0.402, 5%	0.0402, 5%
PC207	NO STUFF	NO STUFF	0.1uF
PC208	NO STUFF	0.1uF	0.1uF
PC209	NO STUFF	NO STUFF	NO STUFF
PR17	8.2K, 0.402, 5%	2.2K, 0.402, 5%	4.7K, 0.402, 5%
PR18	8.45K, 0.402, 1%	NO STUFF	NO STUFF
PR232	NO STUFF	NO STUFF	200K, 0.402, 5%
PR233	NO STUFF	NO STUFF	7.5K, 0.402, 5%
PR234	NO STUFF	NO STUFF	0.0402, 5%
PC23	0.1uF, 0.402, 10V	NO STUFF	200uF, 0.402, 10V
PC24	0.01uF	0.01uF	NO STUFF
PC210	NO STUFF	NO STUFF	130pF, 0.402, 10V
PC211	0.01uF	NO STUFF	NO STUFF
PC153	0.01uF	0.01uF	NO STUFF
PC204	NO STUFF	NO STUFF	51pF, 0.402, 10V
PC206	NO STUFF	NO STUFF	2000pF, 0.402, 10V
PC27	1.0uF, 0.603, 10V	NO STUFF	1.0uF, 0.603, 10V
PC28	0.1uF, 0.402, 10V	NO STUFF	NO STUFF
PR10	10K, 0.402, 1%	10K, 0.402, 1%	NO STUFF
PR7	15.8K, 0.402, 1%	15.8K, 0.402, 1%	NO STUFF
PR229	NO STUFF	NO STUFF	10K, 0.402, 5%
PR5	385K, 0.402, 1%	215K, 0.402, 1%	309K, 0.603, 1%
PD1	CH501H-40PT	NO STUFF	CH501H-40PT
PR6	33, 0.603, 1%	33, 0.603, 1%	NO STUFF
PC11	1.0uF, 0.603, 10V	1.0uF, 0.603, 10V	NO STUFF
PR12	1, 0.603, 1%	0, 0.603, 5%	0, 0.603, 5%
PR16	100, 0.402, 5%	100, 0.402, 5%	0, 0.402, 5%
PC22	220pF, 0.402, 50V	NO STUFF	NO STUFF
PR239	0.0402, 5%	8.45K, 0.402, 1%	8.45K, 0.402, 1%
PC14	0.01uF	0.1uF	0.1uF
PC12	3.3nF	NO STUFF	NO STUFF

TABLE 1							
ADAPTER(W)	TRIP CURRENT (A)	MAX8731A/ISL88731			bq24745		
		R237	R241	R243	R242 (see Note 1)	R241	R243 (see Note 1)
65	3.17	57.6K	13K	105	24.9K	12.4K	205
150	7.43	30.9K	24.9K	499	10.7K	23.7K	499
240	11.69 (see Note 2)	17.8K	6.49K	3.48K	2.37K	8.45K	1.18K
							23.2K

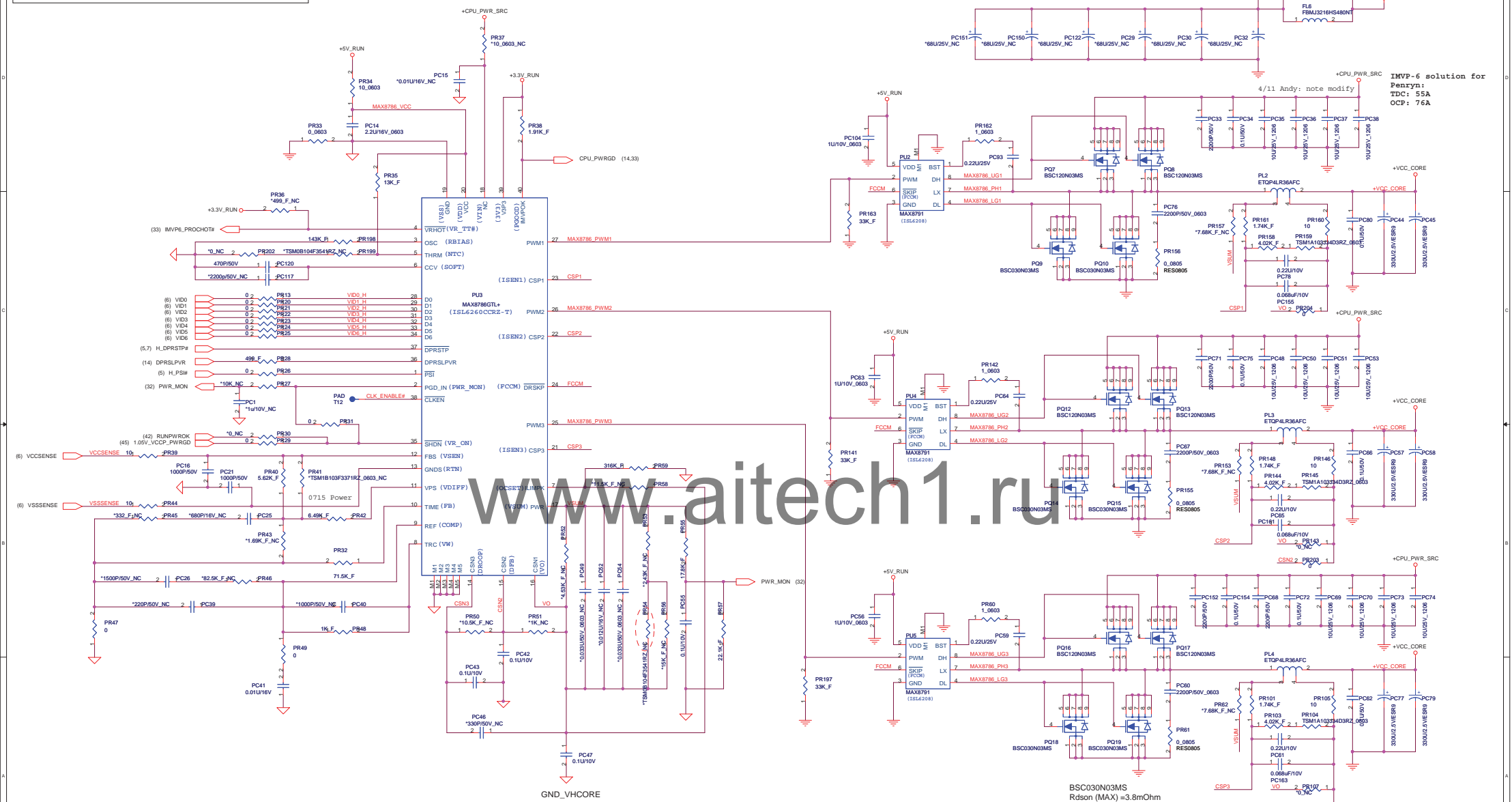
Note 1 : R242 is populated if ADAPT_TRIP_SET is used to program for the next lower adapter
ADAPT_TRIP_SET is floating for the higher adapter, grounded for the lower adapter
Note 2 : RR1 must be 5mOhms instead of 10mOhms for the 240W adapter

Title			Charger (MAX8731)
Size	Document Number	Rev	
Date			Monday, March 06, 2009
Sheet			43 of 61



ADAPT_TRIP_SET:
AC 65W --> H
Battery mode --> H
AC 240W --> L

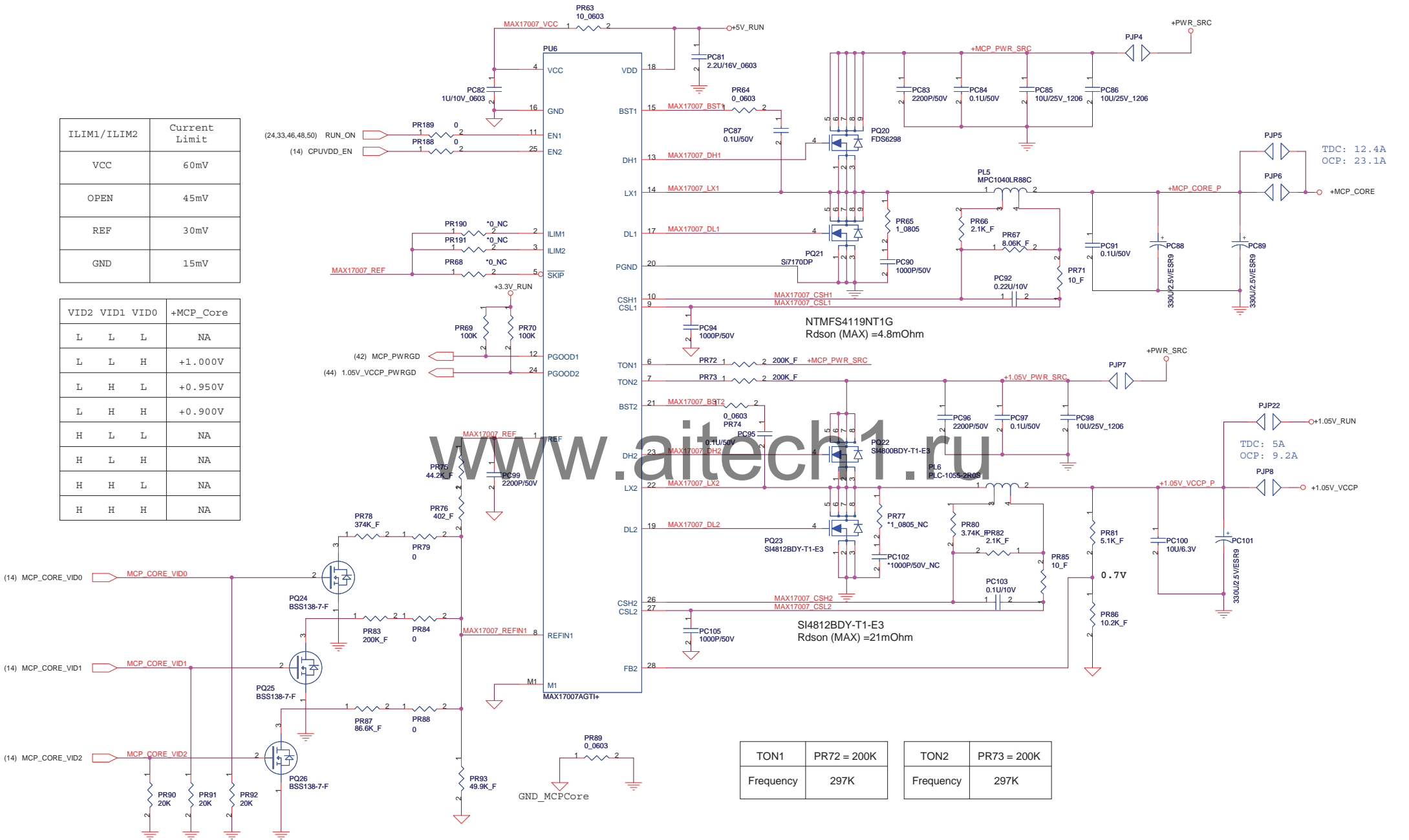
NOTE:
Component Values on Schematic are for MAXIM MAX8786 only.



Title										
CPU_CORE (MAX8786)										
Size		Document Number							Rev	
Dell/FLEX Confidential										A00
Date		Monday, March 09, 2009			Sheet		44		of 61	

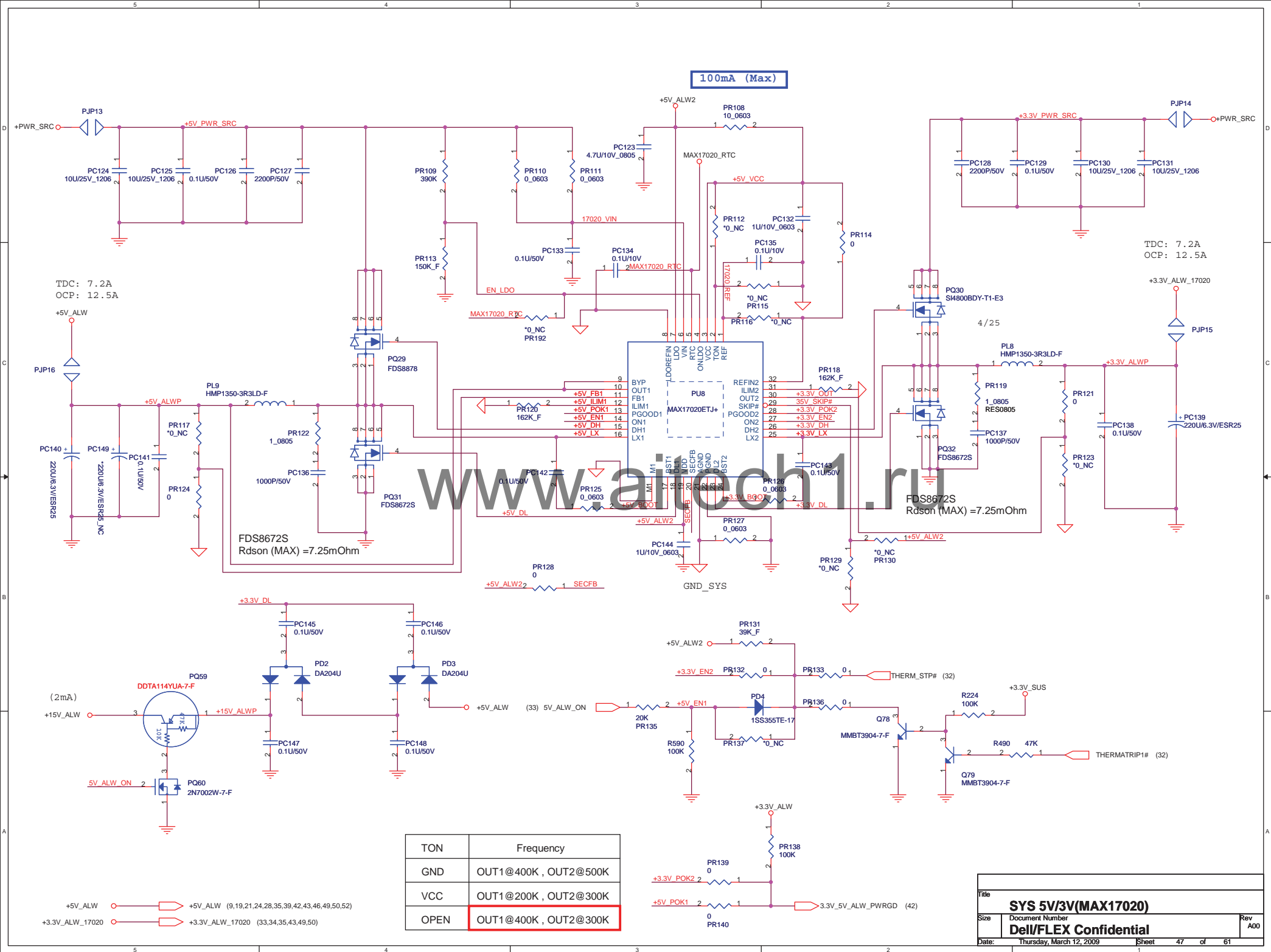
ILIM1/ILIM2	Current Limit
VCC	60mV
OPEN	45mV
REF	30mV
GND	15mV

VID2	VID1	VID0	+MCP_Core
L	L	L	NA
L	L	H	+1.000V
L	H	L	+0.950V
L	H	H	+0.900V
H	L	L	NA
H	L	H	NA
H	H	L	NA
H	H	H	NA



TON1	PR72 = 200K	TON2	PR73 = 200K
Frequency	297K	Frequency	297K

Title			
MCP1.05VCC (MAX17007)			
Size	Document Number	Rev	
	Del/FLEX Confidential	A00	
Date:	Thursday, March 12, 2009	Sheet	45 of 61



100mA (Max)

TDC: 7.2A
OCP: 12.5A

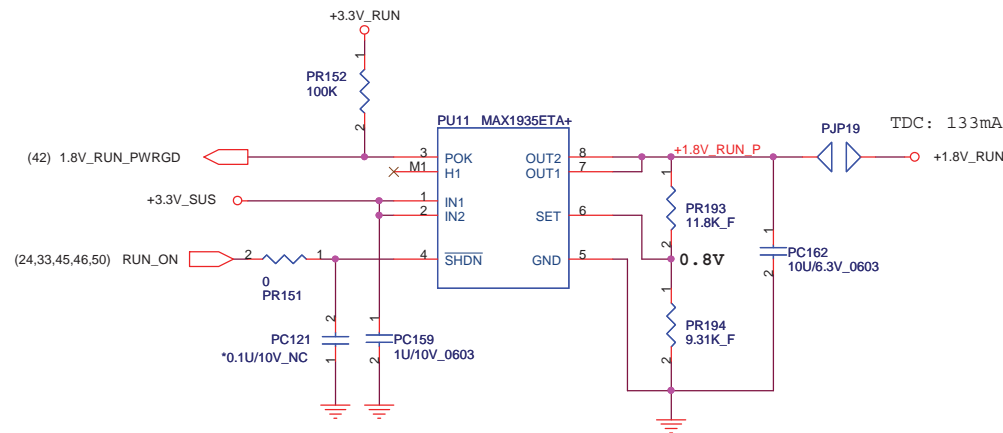
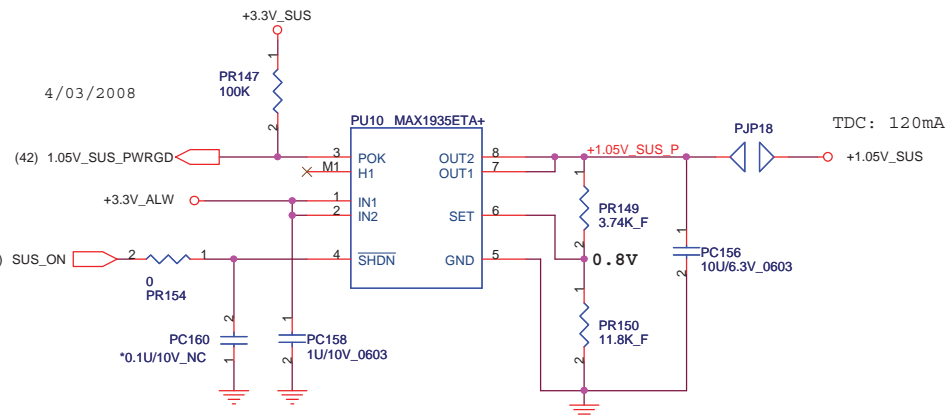
TDC: 7.2A
OCP: 12.5A

FDS8672S
Rdson (MAX) = 7.25mOhm

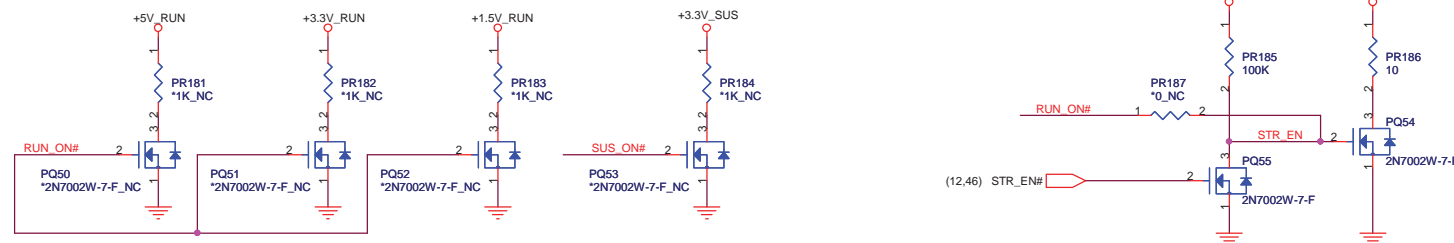
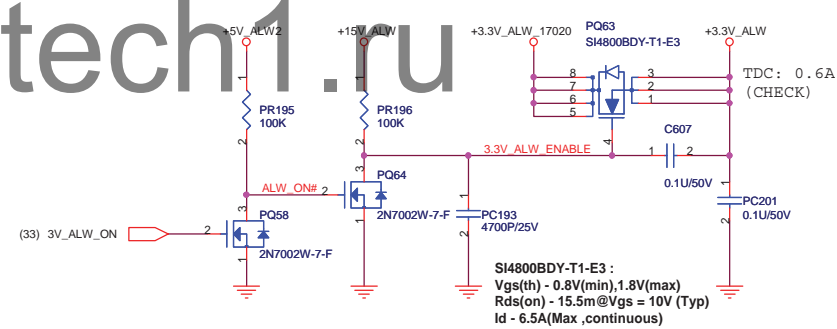
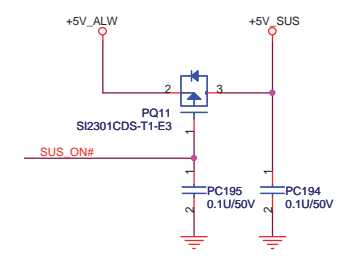
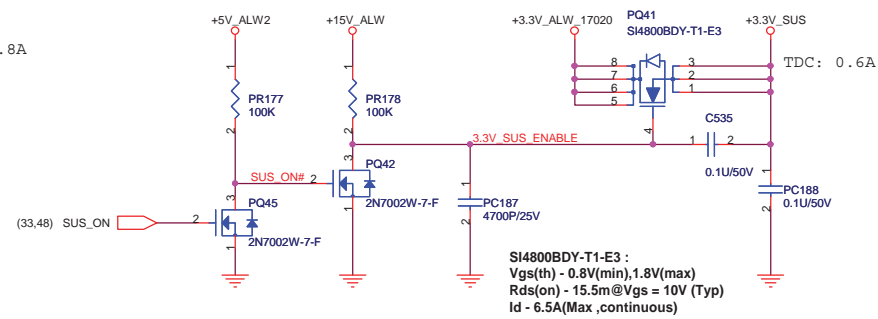
FDS8672S
Rdson (MAX) = 7.25mOhm

TON	Frequency
GND	OUT1@400K , OUT2@500K
VCC	OUT1@200K , OUT2@300K
OPEN	OUT1@400K , OUT2@300K

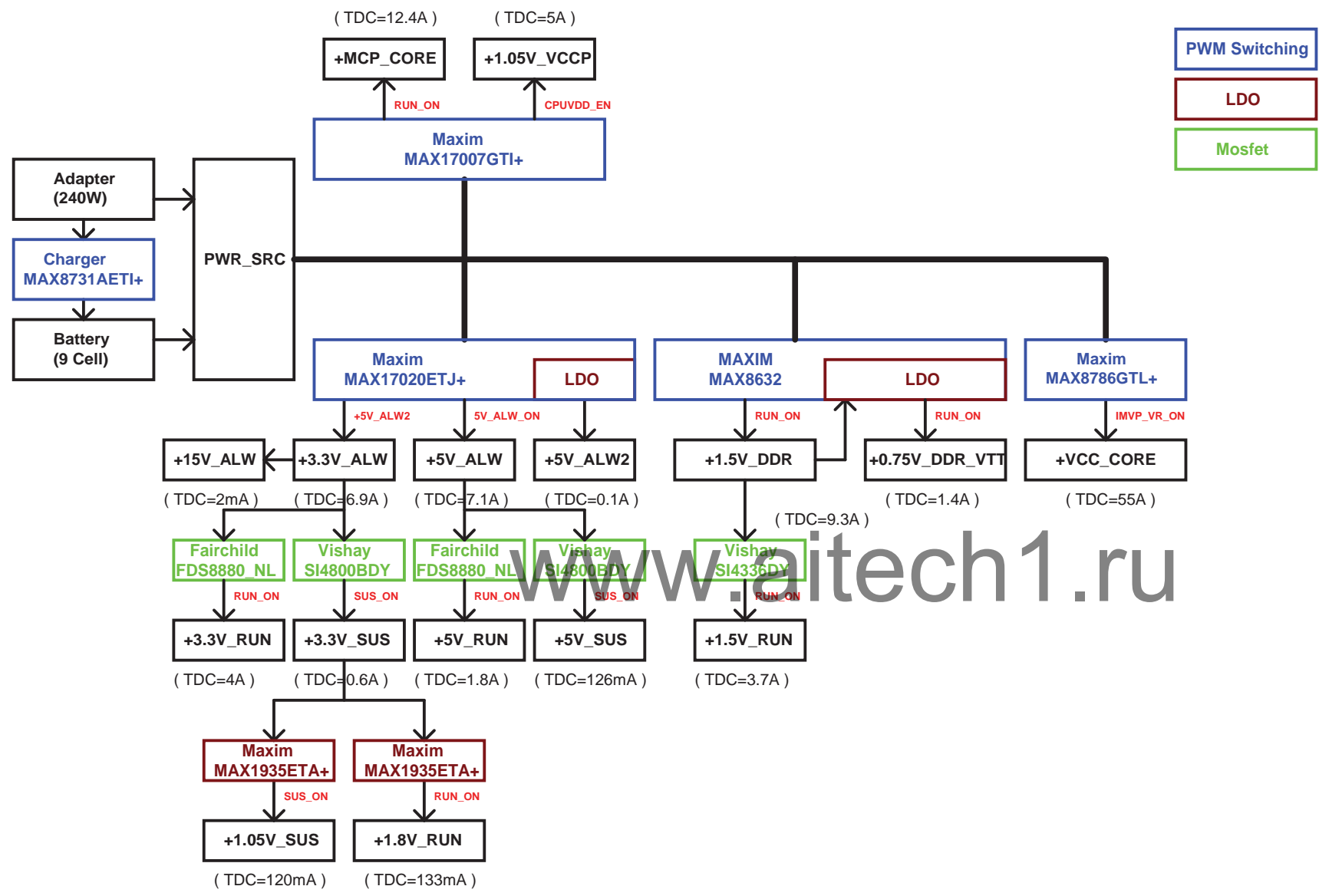
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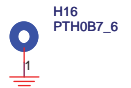
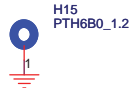
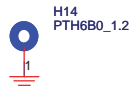
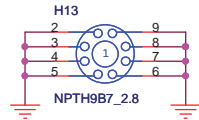
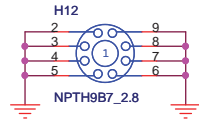
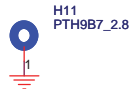
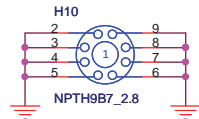
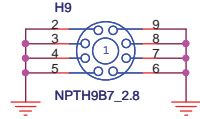
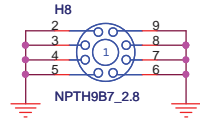
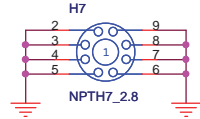
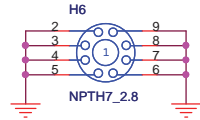
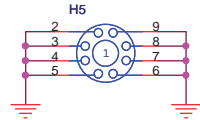
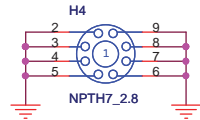
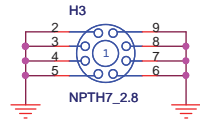
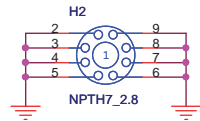
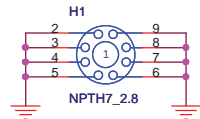
Title		
1.1V_SUS/1.8V_RUN		
Size	Document Number	Rev
Dell Confidential		A00
Date:	Monday, March 09, 2009	Sheet 48 of 61



Title			
RUN POWER SW			
Size	Document Number	Rev	
	Dell/FLEX Confidential	A00	
Date:	Monday, March 09, 2009	Sheet	50 of 61



Screw Hole



FID

FID1
NC, NO CONNECT TO ANY.

FID2
NC, NO CONNECT TO ANY.

FID3
NC, NO CONNECT TO ANY.

FID4
NC, NO CONNECT TO ANY.

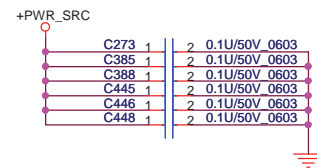
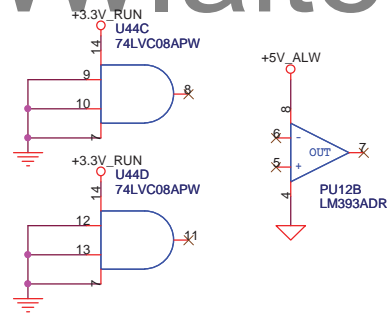
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FID6
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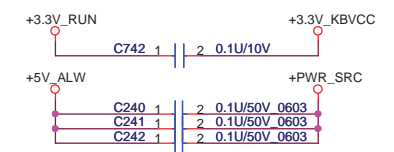
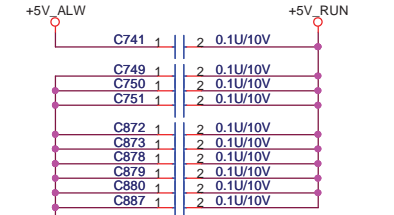
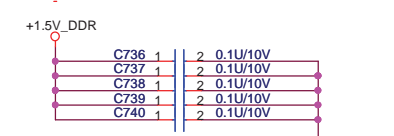
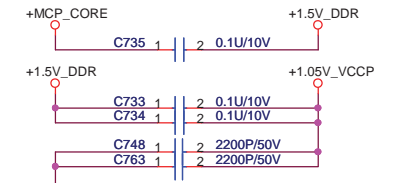
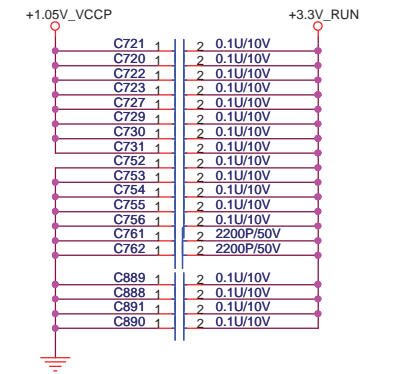
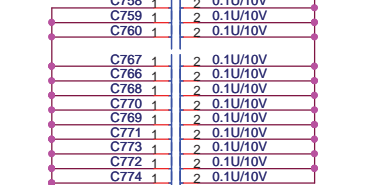
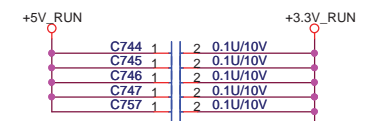
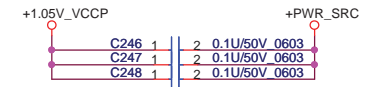
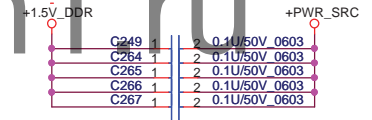
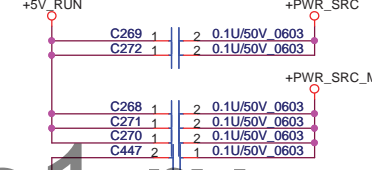
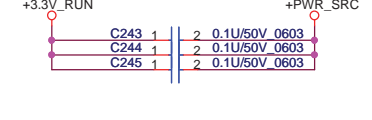
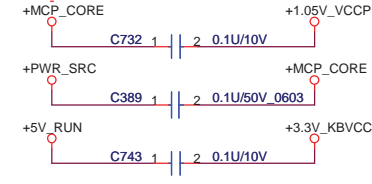
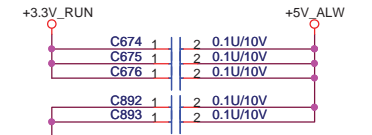
FID7
NC, NO CONNECT TO ANY.

FID8
NC, NO CONNECT TO ANY.

Unused Gate

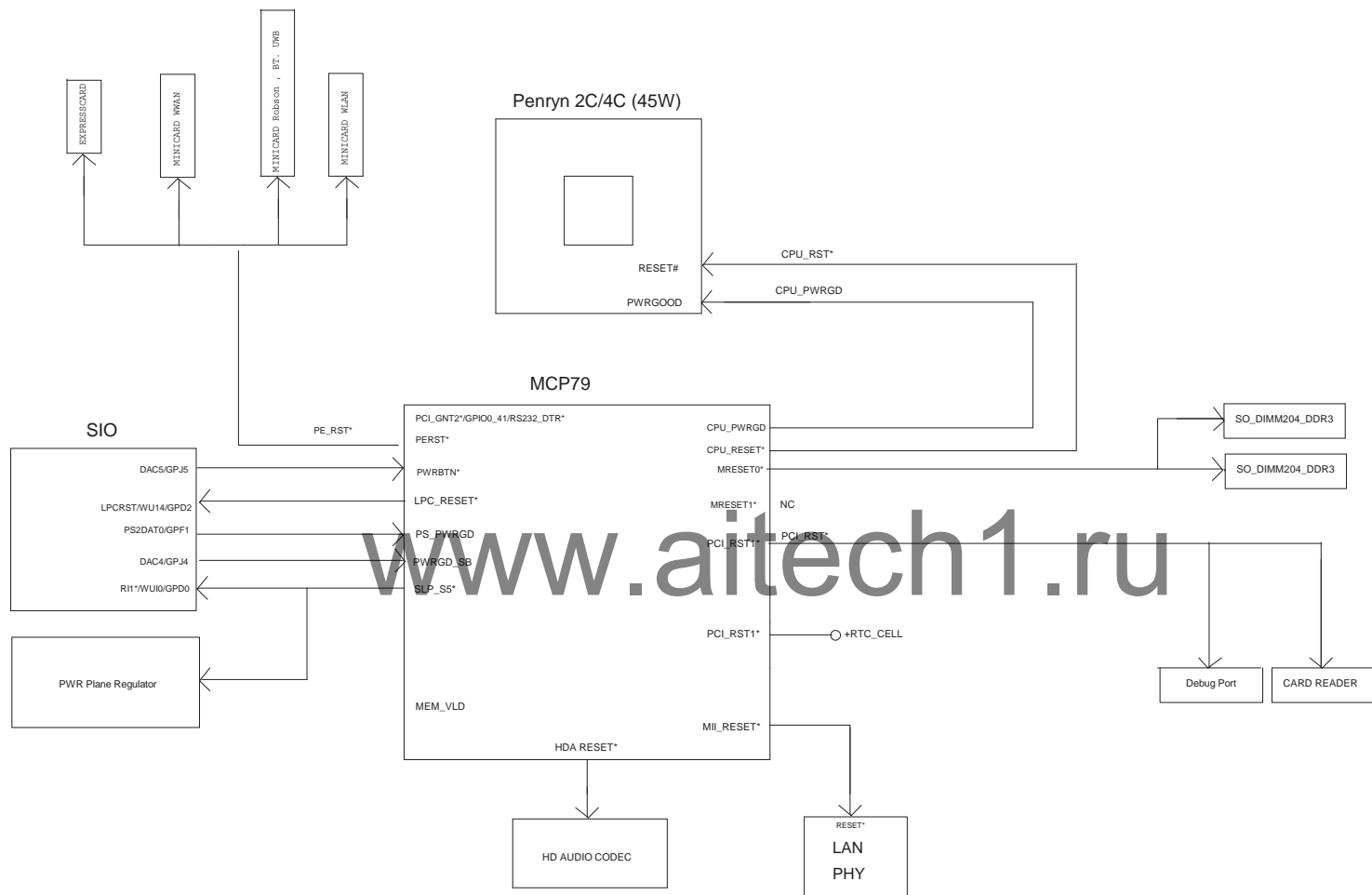


Moat Cap



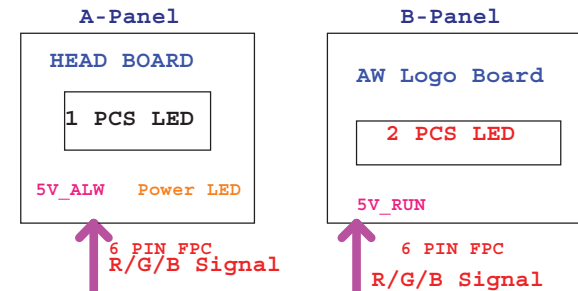
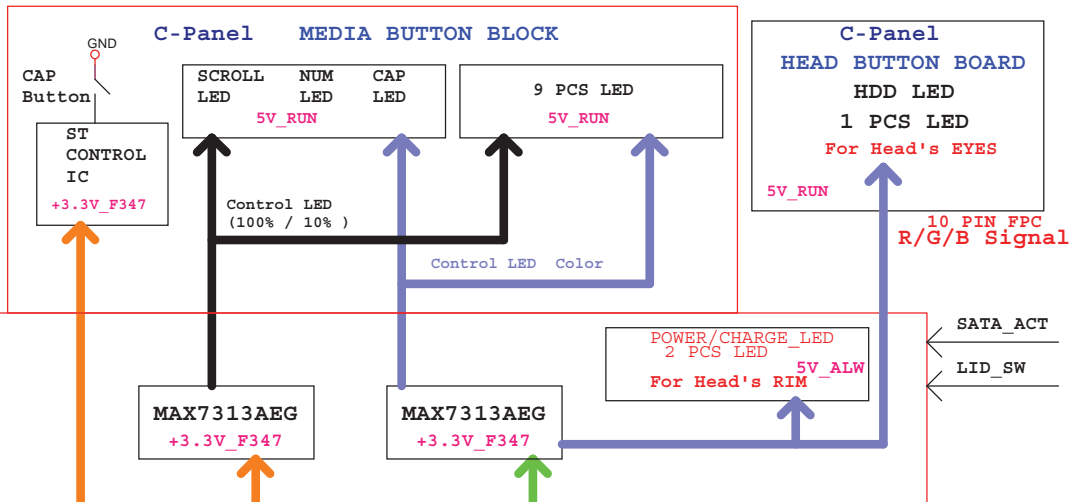
Title			
PAD & SCREW			
Size	Document Number	Rev	
Dell/FLEX Confidential		A00	
Date:	Monday, March 09, 2009	Sheet	52 of 61

RESET MAP



Title			
PCI RESET MAP			
Size	Document Number		Rev
	Dell/FLEX Confidential		A00
Date:	Monday, March 09, 2009	Sheet	53 of 61

Media button board
 1. Play/Pause
 2. Stop
 3. Skip Back
 4. Skip Forward
 5. Vol_DWN
 6. Vol_UP
 7. Wireless On/Off
 8. AW Command
 9. Stealth Mode
 Total: 9 LED



+3.3V_F347 behavior

	State			
	S0	S3	S4	S5
AC In	ON	ON	ON	ON
BAT only	ON	ON	Off	Off

SMBUS

16 PIN FPC

Mother Board

20 Pin Conn

A Head/ B Logo and Webcam Conn

+3.3V_F347 IC C8051F347

3V_ALW

KBC

BT LED Active

MAX7313AEG

+3.3V_F347

MAX7313AEG

+3.3V_F347

R/G/B Signal
6 PIN FPC

5V_RUN
LEFT SPEAKER LED
2 PCS LED

6 PIN FPC

5V_RUN
RIGHT SPEAKER LED
2 PCS LED

R/G/B Signal

16 PIN FPC

5V_RUN
Keyboard LED

TOUCH PAD

4 PCS LED

5V_RUN

12 PIN FPC
R/G/B Signal

Title			LED BOARD		
Size	Document Number				Rev
	Dell/FLEX Confidential				A00
Date:	Monday, March 09, 2009		Sheet	54	of 61

Version change list (P.I.R. List)

Page 1 of 7

Item	Fixed Issue	Reason for Change	Rev	PG#	Modify List	B Ver#	Phast
1	EMI Modify Part of Bead		X00	44, 49	Modify Part of FL5, FL6, FL7, FL8 to BJ3216HS480NT.	X00	SSI
2	Modify Thermal sense Diode	To meet SMSC suggestion in Document AN1214.	X00	5, 6, 9, 32, 42, 49	Modify Q2, Q5, Q22, Q23, Q24, Q25, Q26, Q27, Q28, Q51, Q86, Q88, Q90, Q92, Q94, Q102, Q103, Q111, Q121, PQ37 to MMBT3904-7-F. (From MMST3904, also modify footprint)	X00	SSI
3	Modify ELC parts to NA.	To meet Dell circuit design requirment.	X00	36	1. Modify R637, R638, R639, R640, R641 to NA. 2. Modify Q50, R373, R372, R528, R529, C532, C542, C543, U118 to NA. 3. Modify U45 pin24, R635 pin2, R647 pin2 to +3.3V_ALW. 4. Modify U45 pin22 to LED_CLK, U45 pin23 to LED_DATA. 5. Add CN27 (4 pin debug header)	X00	SSI
4	Modify Footprint of Mini Card.	To separate Wini-lock& Connector	X00	30, 31	Del CN18(MiniCard WLAN Connector)& CN19(MiniCard WWAN, BT, UWB Connector)& CN20(Flash Cache Module Connector) Pin M3,M4,M5,M6.	X00	SSI
5	Move DP AUX pull-up& down resistor.	Modify by NV recommend.	X00	27	Move R191,R200 to CN10(DP conn) side.(NV recommend)	X00	SSI
6	Add LVDS DDC selection pull-up.	Add by NV recommend.	X00	26	Add R520 on U124 pin 1 and pull up to +3.3V_RUN	X00	SSI
7	Seperate Head LED power	To meet Dell circuit design requirment.	X00	24	Modify CN62(CAM/ Head/ Logo Conn) pin11 to +5V_ALW& add C627 decoupling cap	X00	SSI
8	Fine tune MCP power trace.	To increase MCP power trace	X00	7, 9, 10, 13, 14, 15	1. Modify L1 pin1, L2 pin1, L3 pin2, L10 pin1 to +1.05V_VCCP. 2. DEL C427, C57, C62, C121, C122, C432, C174, C311, C217, C204, C214	X00	SSI
9	Modify ELC circuit design	To meet Dell circuit design requirment.	X00	36	1. Modify TP_LED_R_DRV#, TP_LED_G_DRV#, TP_LED_B_DRV# from U43 pin17, 18, 19 to U45 pin17, 18, 19. 2. Modify U51 pin 16 to +5V_ALW, U45 pin 1& 16 to +3.3V_ALW. 3. Modify U45 pin 22& 23 to LED_CLK& LED_DATA.	X00	SSI
10	Modify +1.5V_DDR power sequence	To meet NV power sequence recommend.	X00	46	1. Modify PR95& PR98 to connect "STBY". Also modify PR99 to "SHDN". 2. Modify PR100 to connect "+5V_ALW".	X00	SSI
11	Remove Hardware Total Power control	To solve CPU CLKSTP can't work issue.	X00	7	1. Remove R513 2. Add "H_CLKSTP" to connect MCP79& CPU directly.	X00	SSI
12	Modify Gating parts to NA.	Didn't use these Gating circuit but reserve all of these parts for MXM power gating.	X00	19, 21	Modify Q13, Q15, Q16, Q17, Q36, Q38, Q39, Q40, R189, R190, R248, R249, C310, C312, C313, C324, C326, C333, C334, C365, C366, C367, C368 and C369 to NA.	X00	SSI
13	Update all of connector lists	Update all of connector modification by M.E..	X00	24, 25, 29, 31, 35, 49	Modify footprint of CN7, CN8, CN14, CN16, CN17, CN23, CN52, CN57 and CN62.	X00	SSI
14	Add Moat capacity	Add Moat capacity by EMI request	X00	52	Add C761, C762& C763 Moat capacity by EMI request.	X00	SSI
15	Backlite final-tune.	Add reserve resistor for backlite final-tune.	X00	24	Add R520& R631 (0ohm_0603) for Backlite final-tune.	X00	SSI
16	WebCam DGND	WebCam DGND connect GND directly.	X00	24	Delete C673 to connect GND directly.	X00	SSI
17	Verify BIOS debug pin	Add test pad on Mini card pin 16, 17, 19.	X00	30	Add T29, T31, T32 on CN18 pin 16, 17, 19.	X00	SSI

Title

LED BOARD

Size

Document Number

Rev

Dell/FLEX Confidential

A00

Date:

Monday, March 09, 2009

Sheet

55 of 61

Version change list (P.I.R. List)

Page 2 of 7

Item	Fixed Issue	Reason for Change	Rev	PG#	Modify List	B Ver#	Phast
18	Add 100pF cap near by SIM con.	Verify SIM card DATA& Reset lines.	X00	31	Add C628& C629 to NA and near by CN23.	X00	SSI
19	Connect +V_TV_DAC to GND	Follow NV design guideline	X00	11	Delete R452 and connect it directly to GND.	X00	SSI
20	Modify ELC circuit	To meet Dell circuit design requirment.	X00	36	U42 changes: 1. Change VBUS(pin 8) power to +5V_SUS 2. Change REGIN(pin 7), R632 and R636 pullup to +3.3V_F347. You could use the Q50 circuit for this. 3. Generate +3.3V_F347 from +3V_ALW and control the power state by SUS_ON and ACIN. We need this power to be ON during S0/S3/S4/S5 when on AC. On Battery this power is available only in S3. 4. Connect U40 power to +3.3V_F347 power. 5. Remove all the RGB_OVERRIDE# circuit. 6. Connect LID_SW# to U42 (similar to KB_DET#_R FET circuit) 7. Connect a new GPIO LOW_BATTERY from EC to U42 GPIO. U51: Remove I2C/SMBDAT2 MUX switch. Not required as per new requirement from AlienFX. U43: Change the power to this part to +3.3V_F347 U45 Changes: 1. Change the power to this part to +3.3V_F347 2. Change SCL and SDA connection to I2C_CLK_R, I2C_DAT_R. Change R264, R262, R596 power to +3.3V_F347. Add LID_SW# circuit.	X00	SSI
21	Modify ELC circuit	To meet Dell circuit design requirment.	X00	35	Add R655, Q116, Q117, Q118, Q119 for TP_LED_DRV disable.	X00	SSI
22	Add HDD Power Bulk Capacity	To meet Dell circuit design requirment.	X00	35	Add C630 for HDD 3V power Bulk cap	X00	SSI
23	Improve thermal trip sequence	EMC4002 thermal trip sequence	X00	32	Add C631 for EMC4002 thermal trip sequence.	X00	SSI
24	Add Jumper near by DC Jack	Add Jumper for EMI parts reserve	X00	49	Add PJP12& PJP17 for EMI parts reserve.	X00	SSI
25	Delete S5, S3 pull-high resistor.	Delete EC S5, S3 PH resistor by NV recommend.	X00	33	Delete R380& R383 by NV recommend	X00	SSI
26	Add +5V_SUS gating circuit.	Add +5V_SUS gating circuit for ELC circuit	X00	50	Add PQ11, PC194, PC195 for ELC circuit.	X00	SSI
27	Remove power source cap	Remove it due to space issue.	X00	44	Remove PC31 due to space issue.	X00	SSI
28	Add EMI's modification.	Add EMI's modification.	X00	44	Page11: 1. R75 change from 0ohm to 22ohm. 2. Add 22ohm resistor*4pcs to Net RGMII_TXD0 ,RGMII_TXD1, RGMII_TXD2,RGMII_TXD3 (close to MCP79SLI). Page 14: 1. C177,C173 change from 10pf to 22pf 2. R126,R257 change 0ohm to 22ohm Page24: 1. Mount C568,C569. 2. Modify R415,R416 to L63, L64. 3. Add 0.1uf caps between +5V_RUN and Gnd(close to CN7) for 1 EA (C633) 4. Add 0.1uf caps between +GFX_PWR_SRC and Gnd (close to CN7) for 2 EA (C635, C636) Page28: 1. Mount L27, L28, L46 and leave R300, R301, R302, R304, R394, R395 empty 2. Mount ESD2,ESD3,ESD5. Page 35: 1. Mount CP1,CP2,CP3,CP4,CP5,CP6.	X00	SSI
2. Add 100pf caps*3pcs to Net RSPK_LED_B_DRV# ,RSPK_LED_G_DRV#, RSPK_LED_R_DRV# to GND (close to CN6). (C638, C639, C641) Page 40: 1. Resved a Crystal 25MHz to Lan chip(close to U33) (Y3, C204, C214) 2. C136, C695 change from N/A to 22pf 3. R538, R541 change from 0ohm to 22ohm 4. Add 100pf caps* 3pcs to Net SPD10LDE, SPD100LED, PHY-ACTLED to GND. (C644, C645, C646) 5. Add 0.1uf caps between +3.3PHY and GND for 2 EA. (C764, C765) Page44: Mount PC67, PC76, PC60, R61,PR155,PR156 also change to 0 ohm. Page52: Add 0.1uf caps between 3.3V_RUN and GND for 9 EA. (C766, C767, C768, C769, C770, C771, C772 , C773, C774)							

Title		
History - 2		
Size	Document Number	Rev
Dell/FLEX Confidential		A00
Date:	Monday, March 09, 2009	Sheet 56 of 61

Version change list (P.I.R. List)

Page 3 of 7

Item	Fixed Issue	Reason for Change	Rev	PG#	Modify List	B Ver#	Phast
29	Modify 0603 resistor to JP	Mini-card power consumption more than R327 absorb.	X00	30	Delete R327 and Add JP4 to instead.	X00	SSI
30	Add 3 caps near by Vcore choke	To reduce AC droop	X00	44	Add PC155, PC161, PC163 parallel with PC78, PC65, PC61.	X00	SSI
31	Leave Power resisotr empty	Leave PR41 empty for line load modify	X00	44	Leave PR41 to empty.	X00	SSI
32	Add dampping resistor	Add dampping resistor by Ricoh recommend to final-tune media card signal.	X00	39	Add R504, R505, R534, R535, R638, R656, R657 ,R658 to final-tune Media card signal.	X00	SSI
33	Add PH resistor on display MUX	Add Pull-high resistor by TI recommend.	X00	39	Add R659, R155, R660, R56, R661, R662 pull-high resisotr by TI recommend.	X00	SSI
34	Add TPM circuit	Add TPM circuit by Dell requirement	X00	34	Add U145, R66, R69, R70, R72, R120, R415, RJ5, RJ6, C647, C648, C650, C650, C652, C653 for TPM circuit	X00	SSI
35	Change the MUX source for support Hybrid function	SN74LVC1G3157DCKR repair easier & lower cost than FUSB20.	X00	26	Change MUX source from FUSB20 (10pins) to SN74LVC1G3157DCKR(6pins). The SN74LVC1G3157DCKR amount need double. U120=> U120 & U132 (MXM/MCP LVDS DDC MUX) U121=> U121 & U134 (MXM/MCP VGA DDC MUX) U122=> U122 & U136 (MCP AUX/DDC MUX) U123=> U123 & U138 (MXM/MCP DP AUX MUX) U119=> U119 & U144 (MXM DP AUX/DDC MUX) U126=> U126 & U143 (MXM/MCP HDMI DDC MUX) U124=> U124 & U140 (MCP MEM& LVDS SMBus MUX)	X00	SSI
36	Add test-PAD	Add test-PAD for NV software debug.	X00	12	Add test-PAD on "PCI_REQ2, MXM1_PWR_EN, WLAN_RADIO_DIS#, WLAN_PCIE_RST#, WPAN_PCIE_RST#, WWAN_PCIE_RST#".	X00	SSI
37	Update EMI solution	Update EMI solution	X00	12	Page 29: Add 0.1uF cap between +5V_HDD& GND for 5 EA. (C660, C661, C662, C664, C667). Page 33: 1. R387 change from 0ohm to 22ohm 2. R398 change from N/A to 0ohm 3. C550 change from N/A to 10pf Page 41: Add 0.1uF between GND_LAN& GND and leave empty.	X00	SSI
38	Add Jumper& Modify power plante	Add Jumper& Modify power plante for MXM1 power measurement.	X00	19, 52	1. Add JP20& create +PWR_SRC_MXM1 power. 2. Modify power plante of C315, C316, C317, C318, C319, C320, C268, C270, C271, C447 to +PWR_SRC_MXM1.	X00	SSI
39	Add +5V_RUN_BLOGO power gating	Add +5V_RUN_BLOGO power gating by Dell ELC request.	X00	24	Add Q72, Q123, R96, R327 to gating +5V_RUN and create +5V_RUN_BLOGO power.	X00	SSI
40	Add stitch cap	Add stitch cap between +1.05V_VCCP& GND	X00	10	Add C121, C122 stitch cap fbetween +1.05V_VCCP and GND.	X00	SSI
41	Modify resistor value. (BOM)	Modify the value to meet PCI-E high swing function.	X01	20, 22	Modify R518& R600 to 0 ohm to meet PCI-E high swing function. (MXM card internal pull-high for 10Kohm)	X01	PT
42	eSATA re-drive IC setting	Add components for eSATA re-drive setting	X01	28	Add R663& R664 for eSATA future setting use	X01	PT
43	Revise EC control pin	Remove reserve circuit after double confirm with intel.	X01	5, 6	Page5: Remove R87, Page 6: Remove R689, R690, C798, Q120& Q121 to remove Quad core detect circuit. Page 33: Modify U15 pin 98 to "FUSB31_ON#"& pin 99 to "MXM2_PRESENT#".	X01	PT

Title

History - 3

Size

Document Number

Rev

Dell/FLEX Confidential

A00

Date:

Monday, March 09, 2009

Sheet

57

of

61

Version change list (P.I.R. List)

Page 4 of 7

Item	Fixed Issue	Reason for Change	Rev	PG#	Modify List	B Ver#	Phast
44	Fine tune 1394 signal (BOM)	Fine tune 1394 signal	X01	39	Modify R465, R466, R467& R468 to 54.9ohm.	X01	PT
45	Add Mini-Card card detect resistor	Add pull-high restor for Mini-Card detect	X01	30, 31	Add R380, R383, R402, R416& R452 for Mini-card detect level.	X01	PT
46	Add CAM power control circuit	Driver of CAM can't shut power down	X01	24, 36	Page 24: Add Q73, C668, C311. Page 30: Add R687 pull-high resistor& U41 pin20 for "CAM_PWR_ON"	X01	PT
47	Modify Media Card signal damping resistor. (BOM)	Modify Media Card signal damping resistor for EMI signal fine-tune	X01	39	Modify R504, R505, R534, R535, R638, R656, R657, R658& R482 to 27ohm for EMI signal fine-tune.	X01	PT
48	Improve X'tal timing. (BOM)	To improve X'tal timing by Vendor suggestion.	X01	14, 33, 34	Modify C185, C186, C551& C552 to 15pF and modify C597& C598 to 20pF	X01	PT
49	Fine tune MXM sequence (BOM)	Fine tune MXM power sequence for reliability	X01	32, 42	P32: Delete R223, R224, R530& R374 and Add R607, R608, R487, R488, C794& C795 then connect to "MXM1 35VOK" P42: Modify R567 to 20Kohm and add C775 to GND.	X01	PT
50	Fine tune Media Card signal	Fine tune Media Card signal for EMI& reliability	X01	39	Add R689, R690, R693& R694 (27ohm) for Media Card signal fine tune.	X01	PT
51	For "PEO_PRSENT16#" It need a SW control (MXM_ON#).	When "Hybrid" enabled and MXM_ON# assert to low, 2 of MXM cards PCIECLK will be active.(NV suggest)	X01	10	Stuff R78 and Unstuff R67& R424	X01	PT
52	For GPIO_47 it need to connect "MXM1_PRESENT#"	SBIOS used GPIO_47 to do a judgment whether MXM cards on board.(NV suggestion)	X01	10	Add R141	X01	PT
53	Unstuff DP HPD 100K pull low resistors.	MXM card has internal pull low.Follow MXM3.0 Design guideline.	X01	10, 27	Unstuff R503& R513	X01	PT
54	V_RGB_DAC can be shorted to GND if RGB interface is not used.	Follow MCP79 checklist v08	X01	11	Unstuff L6, C138& C139. Del C137 and Add R87	X01	PT
55	Follow MXM design guideline sequence	Follow MXM design guideline sequence.	X01	19, 21	Modify CN4& CN5 pin27& 280 to +3.3V_RUN. Change C327, C328, C329& C359 pin1 from +3.3V_MXM1(+3.3V_MXM2) to +3.3V_RUN. Modify CN4& CN5 pin1, 3, 5, 7, 9 to +5V_RUN. Change C829, C321, C322, C855, C325, C323, C830, C665, C654, C858, C666& C657 pin1 from +5V_MXM1(+5V_MXM2) to +5V_RUN. Add JP22 to connect +3.3V_MXM1& +3.3V_MXM2.	X01	PT
56	Fix MXM card leakage issue	Add gating circuit to fix leakage issue	X01	19, 20, 22	DEL +3.3V_RUN_HYBRID circuit.(R214,Q78,Q80,R402,C613,Q79,C614,C377) Change +3.3V_RUN_HYBRID power to +3.3V_MXM1(+3.3V_MXM2) . Stuff Q12, R185, Q14, R186, Q104, R500, Q105& R501 Unstuff R201, R582, R639& R640 Stuff Q81, R498, Q82, R499, Q20, R196, Q21& R197 Add D56& D57 Unstuff R641, R652, R653& R654	X01	PT
57	Reserve cap to fine tune sequence	Reserve cap to fine tune PWR_EN sequence	X01	20, 22	Reserve 0.1uf (Unstuff) C766& C777	X01	PT
58	Fix TMDS251 leakage issue	Plug external HDMI device will cause system leakage from TMDS251 vcc pin.	X01	19, 23	Add Q76,C377,C614,C613,C377 and Add net +3.3V_MXM1_HDMI.	X01	PT
59	Update EMI solution of X01 (BOM)	Update EMI solution of X01	X01	40	Modify R683, R684, R685, R686 to 22ohm.	X01	PT

Title		
History - 4		
Size	Document Number	Rev
Dell/FLEX Confidential		A00
Date:	Monday, March 09, 2009	Sheet 58 of 61

Version change list (P.I.R. List)

Page 5 of 7

Item	Fixed Issue	Reason for Change	Rev	PG#	Modify List	B Ver#	Phast
60	Let KBC can judge 2'nd MXM card plug in.	Connect MXM2_PRESENT2# to KBC.Let KBC can judge 2'nd MXM card plug in.	X01	33	MXM2_PRESENT2# connect to U15 pin 99.	X01	PT
61	Fix press 4 second shutdown leakage issue.	Crt_Ddc_Sel (GPIO36), Dp_Sel(GPIO4), Lvds_Sel(GPIO 20), Lvds_Ddc_Sel(GPIO 21), Lvds_Mem_Ddc_Sel (GPIO6), HDMI_DDC_Sel(GPIO5) active high after press 4 second shutdown then cause leakage to +3V_RUN.	X01	23, 26	Add pull high resistors & diodes. R695, R696, R697, R698, R699, D44, D47, D48, D54, D49& D55	X01	PT
62	Delay MXM1_35VOK sequence (BOM)	Delay MXM1_35VOK sequence to control MXM thermaltrip gating.	X01	42	Add C775 Change R567 to 20K	X01	PT
63	Delete HDMI pass resistor	Remove them to improve HDMI signal	X01	23	Remove R485, R486, R487, R488, R489, R490, R491, R492, R493, R607& R608.	X01	PT
64	Add cap near by Media card controller	Add cap to improve Media card signal	X01	39	Add C217, C778, C779, C780, C781, C782, C785, C786, C787, C788, C789, C790, C791& C792	X01	PT
65	Meet SMSC EMC4002 circuit design (BOM)	Add circuit to meet SMSC suggest, also keep Dell request.	X01	32, 47	Modify R218 to 4.7K ohm and pull-high power to +3.3V_SUS Add Q78, Q79, R224& R490.	X01	PT
66	Add Dampning resistor	Add 22 ohm resistor to improve CRT signal	X01	25	Add R374& R485	X01	PT
67	Fix Keyboard LED wrong color	In order to correct keyboard LED display	X01	37	Swap CN57 pin 3, 4 pin define from R to G& G to R.	X01	PT
68	Follow NV designguide (BOM)	Modify schematic to meet NV design guideline	X01	9, 10, 11, 13, 14, 15	Modify C115, C123, C131, C161, C164, C191, C196& C198 to 2.2uF. Unstuff R100 Modify R145, R146, R211& R244 to 2.2Kohm. Modify C116 to 2.2uF. Add C65, C174& C793	X01	PT
69	Update EMI solution of X01	Update EMI solution of X01	X01	11, 19, 24, 28, 32, 35, 39, 40, 47, 49, 52	Unstuff R82, R469, R470, R471, R474, R541& C136 Stuff C204, C214, C835, C836, C837, C838, L39, L40& Y3. Add C796, C797, C798, C799, C800, C801, C802, C803, C804, C805, C806, C807, C824, C825, C864, C865, C866, C867, C869, C870, C871, C872, C873, C874, C878, C879, C880, C887, C888, C889, C890, C891, C892, C893. Move C677, C678, C679, C680, C681, C682, C683& C684 to near by CN63. Delete R549 and Add C894.	X01	PT
71	Power VDS derating modify	To meet Power VDS derating specification	X01	45, 46, 47	Stuff PR65, PR96, PR119, PR122& PC90. Stuff PC118, PC136& PC137 and modify them to 1000pF	X01	PT
72	Improve AC-in Detect function	Due to MXM had internal pull-high at AC-in signal cause AC-in detection fail	X01	19	Add R491& Q120 and R502 to 100Kohm	X01	PT
73	Update eSATA re-drives& FSUSB31K8X IC setting (BOM)	Due to eSATA re-drive IC set to increase signal stress cause signal failure and FSUSB31K8X setting.	X01	28	Stuff R663& R664 and Unstuff R618& R619 for eSATA re-drive IC. Stuff R489 for FSUSB31K8X.	X01	PT
74	Reserve SIM card connector and stuff components to test FCM mini card connector (BOM)	In order to prepare reserve CN19 so stuff all of components for FCM and reserve SIM card connector	X01	31	Unstuff CN23, C523, C524, C525, C526, C527& ESD4. Stuff R333, R334, R335, R336, R337 R338, R339, R349, R351, R353& R355.	X01	PT

Title

History - 5

Size

Document Number

Rev

Dell/FLEX Confidential

A00

Date:

Monday, March 09, 2009

Sheet

59 of 61

Version change list (P.I.R. List)

Page 6 of 7

Item	Fixed Issue	Reason for Change	Rev	PG#	Modify List	B Ver#	Phast
75	Fine tune PCI clock (BOM)	Due to PCI clock fail of EA test report.	X01	12	Stuff C151 and modify to 15pF	X01	PT
76	Reserve unused MXM2 power sequence control circuit (BOM)	Reserve unused MXM2 power sequence control circuit	X01	42	Unstuff C724, C725, C726, C728, D45, D46, R611, R612, R613, R642, R643, R644, R645, Q100, Q101, Q102& Q103.	X01	PT
77	CRT signal improvement (BOM)	To improve CRT signal	X01	25	Modify L56, L57& L58 to BLM18BB750SN1D	X01	PT
78	Turn off SUS power in DC mode	Turn off SUS power in DC mode to prevent leakage current	X01	32, 33, 42	Modify R205 pin 1 to +3.3V_SUS. Add R492 and unstuff. Modify U15 pin 85 to "RUNPWROK#" and delete R590& Q77.	X01	PT
79	MCP79 Vcore table modify	To meet NV MCP79 designguide - DG-03328-001_v12	X01	45	Modify PR83 to 200Kohm_F. Also modify MCP79 Vcore table.	X01	PT
80	DP HPD floating (BOM)	R513 avoid DP HPD floating	X02	27	Mount R513	X02	ST
81	DP power drop too big (BOM also)	Avoid DP power drop cause by D17.	X02	27	Add R549 (0ohm_0603) and leave D17 NC.	X02	ST
82	DP leakage current issue (BOM)	Avoid DP leakage current	X02	27	Modify D33 from BAV99-7-F to RB500V-40.	X02	ST
83	HDMI TV leakage issue	Fix HDMI TV plug -in leakage from TMDS251 to system.	X02	19	Add Q77 (2N7002) for dis-charge.	X02	ST
84	Meet new inductor's droop voltage (BOM)	Meet new inductor's droop voltage	X02	44	Modify PL2, PL3, PL4 to ETQP4LR36WFC. Modify PR40& PR59 to 5.63Kohm & 316Kohm.	X02	ST
85	Media Board sometimes fail (BOM)	Improve SM bus fan-out ability for Media board	X02	22, 33	Modify R196, R197, R273, R274 to 13Kohm	X02	ST
86	EMI solution in ST phase - 1. (BOM)	Add EMI solution	X02	28, 41	Add EMI2& EMI3. Mounted L32, L42, L43& L45 and remove R366, R371, R375, R381, R382, R411, R412& R414 by BOM change.	X02	ST
87	AMD MXM leakage current issue	Avoid AMD MXM leakage current	X02	20, 22	Add D60& D61 and Delete R640& R652.	X02	ST
88	SM bus equivalent parallel resistance low (BOM)	SM bus equivalent parallel resistance too low so increase the value of resistor	X02	23, 26	Modify R494, R495, R496, R497, R601& R604 to 10Kohm in page 23. Modify R147, R155, R156, R609, R610, R627, R659, R660, R661& R662 to 10Kohm in page 26.	X02	ST
89	eSATA output driving strength (BOM)	Improve eSATA output driving strength	X02	28	R618, R619 Mount and R663, R664 NA.	X02	ST
90	Fine tune +3.3V_MXM1 power sequence (BOM)	Fine tune +3.3V_MXM1 power sequence to close 3V of MXM card's power sequence	X02	28	C310,C312,C614 change to NA	X02	ST
91	Fine tune MXM card power enable sequence (BOM)	Fine tune MXM card power enable sequence make sure +3.3V_MXM1 power sequence to close 3V of MXM card's power sequence	X02	20, 22	R192,R256 change to 10Kohm C776,C777 Mount.	X02	ST
92	Follow TI vendor suggestion	To make sure the TMDS 251 power stable	X02	23	Add 10UF on +3.3V_MXM1_HDMI	X02	ST
93	Reserve unused power (Audio board)	Reserve unused power for Media card of Audio board	X02	39	Add 0ohm and leave empty.	X02	ST

Title

History - 6

Size

Document Number

Rev

Dell/FLEX Confidential

A00

Date:

Monday, March 09, 2009

Sheet

60

of

61

Version change list (P.I.R. List)

Page 7 of 7

Item	Fixed Issue	Reason for Change	Rev	PG#	Modify List	B Ver#	Phast
94	Fine tune +3.3V_MXM1& +5V_MXM1 power sequence (BOM)	Fine tune +3.3V_MXM1& +5V_MXM1 power sequence .	X02	19	Stuff R176& Unstuff R486	X02	ST
95	USB waveform fail	Improve USB waveform	X02	28	Stuff R394, R395& Unstuff L46, ESD5	X02	ST
96	VGA ACAVIN control (BOM)	Add VGA ACAVIN	X02	19	Add Q80 and connect to ADAPT_TRIP_SET. Modify R502 to 4.7Kohm.	X02	ST
97	3.3V OCP keeping re-try (BOM)	Make sure signal won't floating and keep original request	X02	47	Modify PR135 to 20K Add R590	X02	ST
98	EMI solution in ST phase - 2. (BOM)	Add EMI solution	X02	39	C792 change from 10pf to 15pf R482 change from 27ohm to 0ohm	X02	ST
99	Media Card signal waveform improve	Media Card signal waveform improve	X02	39	R118, R504, R505, R534, R535, R638, R656, R657, R658, R689, R690, R693& R694 change from 27ohm to 33ohm Unmoute C217, C778, C779, C780, C781, C782, C785, C786, C787, C788, C789, C790, C791& C792.	X02	ST
100	1.5V power regulator level modify (BOM)	Modify 1.5V power regulator level	A00	46	Modify PR221 to 80.6Kohm	A00	MP
101	Fix 1.5V power non-modification (BOM)	Fix 1.5V power non-modification	A00	46	PR214& PR221 un-stuff	A00	MP
102	Fine tune +3.3V_MXM1& +5V_MXM1 power sequence (BOM)	Fine tune +3.3V_MXM1& +5V_MXM1 power sequence .	A00	19	Unstuff R176& stuff R486	A00	MP
103	Fine tune MXM card power enable sequence (BOM)	Fine tune MXM card power enable sequence make sure +3.3V_MXM1 power sequence to close 3V of MXM card's power sequence	A00	20, 22	R192, R256 change to 0ohm C776, C777 Unstuff.	A00	MP
104	Modify Display Port HPD vlotage sense.	Modify Display Port HPD vlotage sense to meet NV checklist	A00	27	Modify R65 to 1Kohm	A00	MP

Title

History - 7

Size

Document Number

Rev

Dell/FLEX Confidential

A00

Date:

Monday, March 09, 2009

Sheet

61 of 61